DPA-Switch

| Application | Device | Power Output | Input Voltage | Output Voltage | Topology |
| :--- | :--- | :--- | :--- | :--- | :--- |
| DC-DC Converter | DPA423R | 5 W | $36-75 \mathrm{VDC}$ | 5 V | Flyback |

## Design Highlights

- Small footprint: $35 \mathrm{~mm} \times 20 \mathrm{~mm}$ (1.4 in. $\times 0.8$ in.)
- High efficiency flyback (>80\% min.)
- 8.8 W per cu. in.
- Low component count
- Accurate line OV and UV protection
- Thermal, short circuit and output overload protection
- No current sense components


## Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. Resistor R1 sets the input under/over voltages to 33 V and 86 V , respectively. Including tolerances, these thresholds guarantee the converter is operational between 36 V and 75 V without the cost of additional line sense components. Resistor R3
programs the internal current limit of the DPA423R to 53\% of nominal. This limits the overload power that can be delivered in a fault condition.

Zener VR1 clamps the leakage inductance spikes to keep the DRAIN voltage at a safe level. The bias supply for U1 is provided from the auxiliary flyback transformer winding (pins 2 and 4), rectified and filtered by diode D1 and capacitor C23.

A snubber for diode D2 (capacitor and resistor) can be used, but was not needed in this application. Inductor L2 and capacitor C12 form a post filter to reduce high frequency output switching ripple. A soft-finish network, C18, D3 and R7, eliminates output turn-on overshoot. The remaining components provide output voltage regulation and loop compensation.


## Key Design Points

- For the nominal under-voltage set point $\mathrm{V}_{\mathrm{UV}}$ :
- $\mathrm{R} 1=\left(\mathrm{V}_{\mathrm{uv}}-2.35\right) / 50 \mu \mathrm{~A}$

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\mathrm{V}_{\mathrm{ov}}=(\mathrm{R} 1 \times 135 \mu \mathrm{~A})+2.5 \mathrm{~V}
$$

- For highest efficiency designs: use continuous conduction mode operation designed at approximately $0.4 \mathrm{~K}_{\mathrm{RP}}$; minimize turns in the transformer while keeping AC flux density (BM) $<3000$ Gauss; fully fill a single layer for each winding to minimize leakage inductance and maximize copper fill factor; use a Schottky rectifying diode (D2) with a low forward drop (in this case, the SL23 diode has a $\mathrm{V}_{\mathrm{f}}=0.320 \mathrm{~V}$ at $125^{\circ} \mathrm{C} / 2 \mathrm{~A}$ ).
- Resistor R3: the PIXIs spreadsheet calculates the peak current (IP) of the power supply. Resistor R3 is chosen to set the


Figure 2. Efficiency vs. Output Power.
internal current limit 10\% to 15\% above the calculated IP value. This limits overload power (worst case is at high input line).

- Set resonant frequency of post-filter (L2, C12) beyond crossover frequency (typically $5 \%$ to $10 \%$ of switching frequency).
- For main secondary current loop from transformer pin 8 to diode D2 and capacitors C10, C11 and back to pin 6 of the transformer: ensure identical path length for C10 and C11 to guarantee they equally share the ripple current.
- Due to the very tight size constraints on this power supply, the drain voltage traces should be kept as short as possible and where possible, shielded by surrounding them with source potential traces. This will prevent noise coupling to the lowvoltage signal pins of the DPA-Switch.

| Transformer Parameters |  |
| :--- | :--- |
| Core Material | EFD-10 Ferroxcube 3F3, AL of $100 \mathrm{nH} / \mathrm{T}^{2}$ |
| Bobbin | EDF-10 8 pin (or equivalent) |
| Winding Order <br> (pin numbers) | $1 / 2$ Primary: (1-FL), tape <br> Bias: (4-3), $5 \mathrm{~V}(5-8)$, tape <br> $1 / 2$ Primary: (FL-2), tape |
| Primary Inductance | $174 \mu \mathrm{H}, \pm 10 \%$ |
| Primary Resonant <br> Frequency | 4.7 MHz (minimum) |
| Leakage <br> Inductance | $1.0 \mu \mathrm{H}$ (maximum) |

Table 1. Transformer Parameters.

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