Design Example Report

Title	*10 W, 15 V_{DC} Output Non-Isolated Automotive Power Supply for 400 V Systems Using LinkSwitch™-TN2Q LNK3209GQ*
Specification	60 V_{DC} – 550 V_{DC} Input; 15 V_{DC} / 0.65 A Output
Application	Non-Isolated Automotive Auxiliary Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-965Q
Date	July 31, 2023
Revision	2.0

Summary and Features

- Highly integrated solution for 400 V_{DC} non-isolated BEV automotive applications
- Low component count design (26 total components; including connectors, heat sink, and thermal pads)
- Wide range input from 60 V_{DC} to 550 V_{DC}
- ≥75 % full load efficiency across input voltage range
- <±5 % line and load regulation
- Ambient operating temperature from -40 °C to 105 °C
- Fully fault protected including output current limit and short-circuit protection
- Uses automotive qualified AEC-Q surface mount (SMD) components

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Disclaimer:

1 Introduction

This engineering report describes a 10 W non-isolated automotive power supply designed to provide a nominal output voltage of 15 V_{DC} at a maximum load of 650 mA. It is intended for use in 400 V battery system electric vehicles. Typical applications include auxiliary supplies for active discharge blocks within onboard chargers or traction inverters, pyro disconnect in battery packs, control power for HVAC compressors, PTC auxiliary heaters, and body control modules.

This design utilizes the LNK3209GQ from the LinkSwitch-TN2Q family of automotive ICs.

The design provides functional isolation by observing the creepage and clearance requirements as indicated in IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

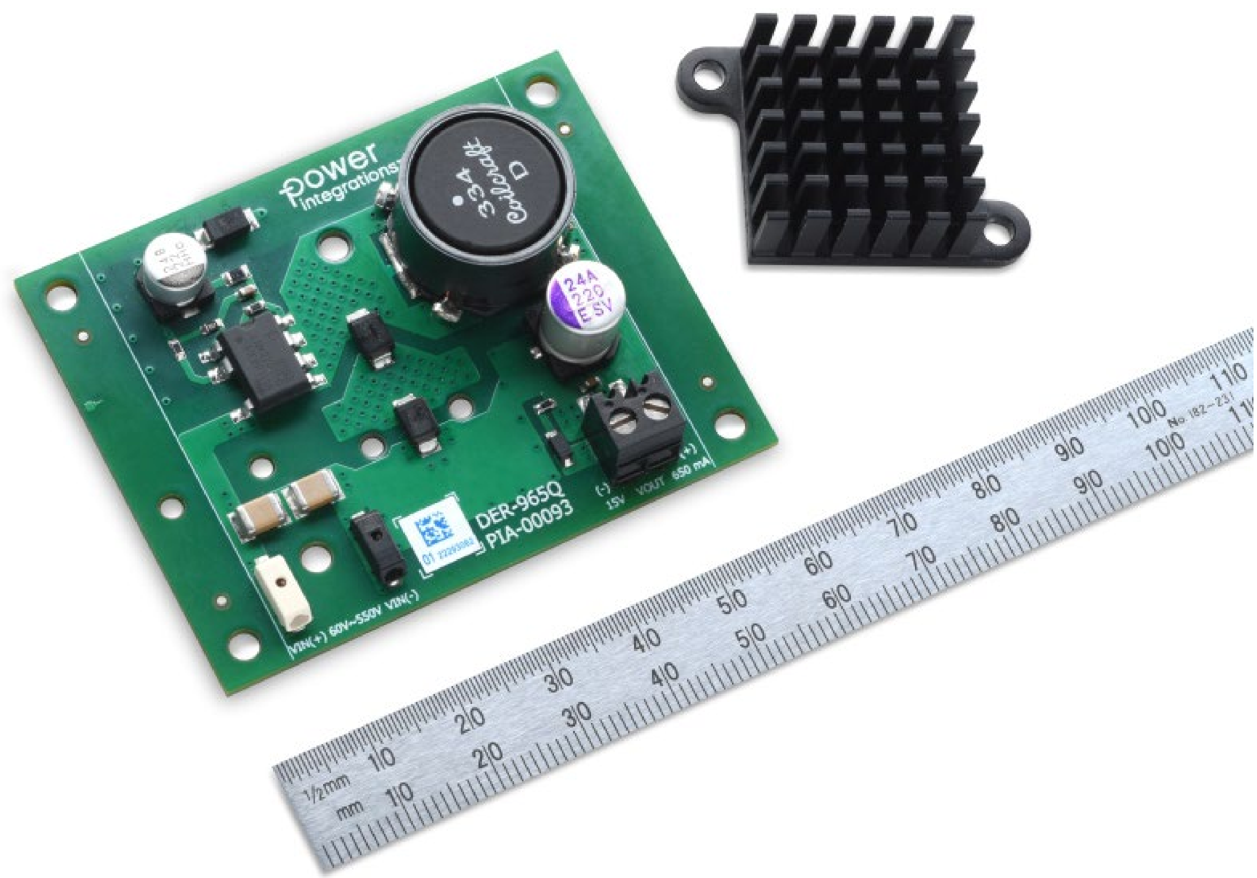


Figure 1 – Populated Circuit Board, Entire Assembly.

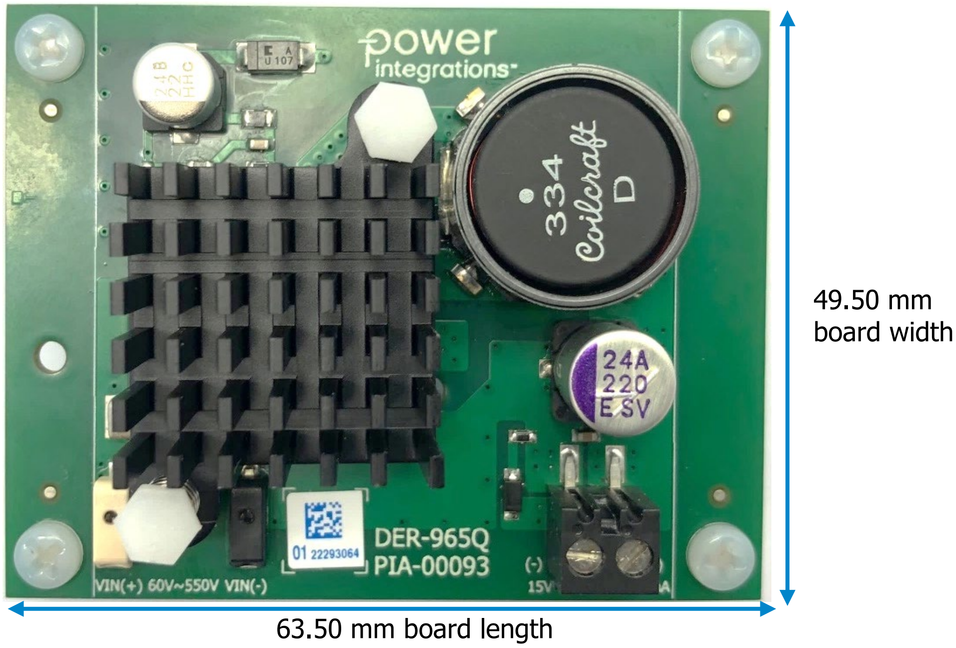


Figure 2 – Populated Circuit Board with Heat Sink - Top.

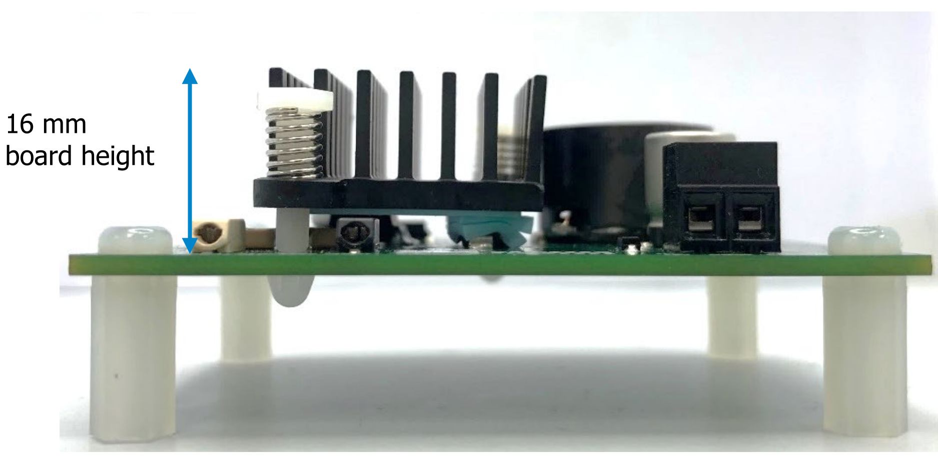


Figure 3 – Populated Circuit Board with Heat Sink - Side.

2 Design Specification

The following tables below represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV - Switching Operation Conditions	**HV**	60	400	550	V_{DC}
Operating Switching Frequency	$\mathbf{f_{SW}}$			70	kHz
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	$\mathbf{V_{OUT}}$	14.25	15	15.75	V_{DC}
No Load Output Voltage				18.5	
Output Voltage Load and Line Regulation[1]	$\mathbf{V_{REG}}$	-5		+5	%
Ripple Voltage Measured on Board	$\mathbf{V_{RIPPLE}}$			240	mV
Output Current Parameters					
Output Current	$\mathbf{I_{OUT}}$	65		650	mA
Output Power Parameters					
Continuous Output Power at 60 V_{DC} – 550 V_{DC} Input	$\mathbf{P_{OUT}}$		9.75	10	W
Output Overshoot and Undershoot During Dynamic Load Condition	$\mathbf{\Delta\ V_{OUT}}$			10	%

Table 1 – Electrical Specifications.

[1] Not including no load condition.

2.2 Isolation Coordination

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of LNK3209GQ	BV_{DSS}			750	V
System Voltage	V_{System}			530	V
Working Voltage	V_{RMS}			550	V
Pollution Degree	PD			2	
CTI for FR4	CTI	175		399	
Altitude Correction Factor for h_a = 5500 m	c_{ha}			1.59	
Technical Cleanliness Requirement				1.0	mm
Clearance Distance Requirement	CLR	3.4			mm
Creepage Distance Requirement	CPG	4.2			mm

Table 2 – Isolation Coordination[2].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_a	-40		105	°C
Altitude of Operation	h_a			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

[2] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

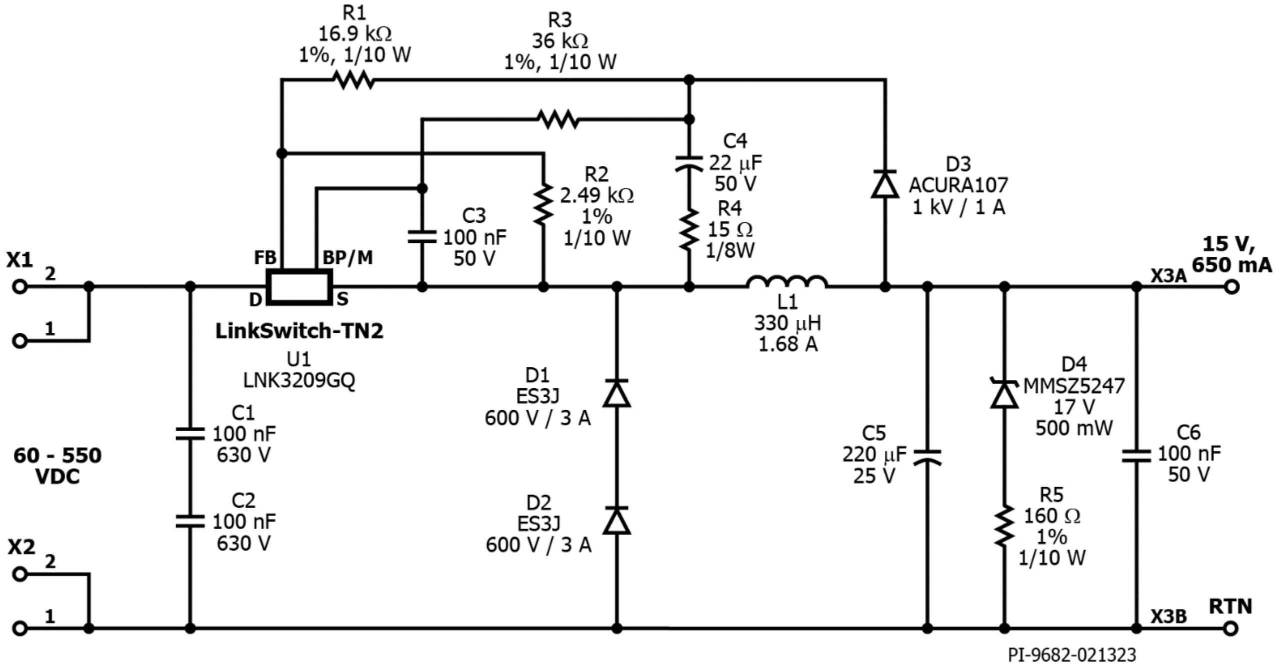


Figure 4 – DER-965Q Schematic.

4 Circuit Description

The design uses the LNK3209GQ IC in a high side drive buck converter. The circuit provides a non-isolated 15 V_{DC}, 650 mA continuous output up to 85 °C ambient temperature for the entire input range of 60 to 550 V_{DC}. At 105 °C ambient temperature, the full 10 W can be delivered from 60 V to 400 V input and a derated 8.25 W at 550 V_{DC} input.

The LinkSwitch-TN2Q family of ICs for automotive power supplies provides significant reduction in component count compared to traditional discrete solutions. Regulation is achieved using a low-cost resistor divider feedback network. The switching frequency jitter feature of the LinkSwitch-TN2Q family and the 66 kHz switching frequency of operation helps reduce EMI. Each device incorporates a 750 V power MOSFET, oscillator, On/Off control, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and overvoltage protection circuitry onto a monolithic IC. A full suite of protection features enables safe and reliable power supplies; protecting the device and the system against device over-temperature faults, lost regulation, and power supply output overload or short-circuit faults.

4.1 Input Filter

Bypass capacitors C1 and C2 placed near the LinkSwitch-TN2Q IC provides local instantaneous charge and a stable DC bus to the buck converter. These were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

NOTE: No dv/dt or inrush current limitation is provided. If the input is directly connected to HV DC (e.g., directly to the HV traction battery) without a pre-charge stage, then adding a series impedance is recommended to prevent damage to the ceramic input capacitors. The impedance should limit the peak capacitor dv/dt to <8 kV / μs or as recommended by the capacitor manufacturer. The impedance can be either a discrete resistor or from part of the parasitic resistance of other components e.g., filter inductors. The use of an input resistor can also function as a fusing element to protect against failure of the power supply. Values in the range of 1-10 ohms are typical, though it is common to have multiple parts in series such that the voltage rating of each resistor is not exceeded.

4.2 Power Stage

The LinkSwitch-TN2Q automotive IC, freewheeling diodes D1 and D2, output inductor L1, and output capacitor C5, forms the power stage.

The LNK3209GQ IC is self-starting from the DRAIN (D) pin with local supply decoupling provided by capacitor C3 connected to the BYPASS (BP/M) pin when the input is first applied. During normal operation the IC is powered from the output via resistor R3. R3 is selected to allow the minimum current required by the IC as stated in the datasheet. The design operates in mostly continuous mode (MCM) due to the output load current requirement. The peak L1 inductor current is set by the LNK3209GQ internal current limit. The control scheme used is ON/OFF control. The switch on-time for every switching cycle is determined by the inductance value of L1, LinkSwitch-TN2Q current limit, and the high voltage DC input. Output regulation is accomplished by skipping switching cycles depending on the feedback signal applied to the FEEDBACK (FB) pin. This differs significantly from the traditional PWM schemes that control the duty cycle of each switching cycle.

4.3 Output Rectification

During the ON time of IC1, the current ramps due to L1 and is simultaneously delivered to the load. During the OFF time, the high voltage supply is cut off and the inductor current ramps down via the path provided by the freewheeling diodes D1 and D2 and is delivered to the load. Diodes D1 and D2 are selected as ultrafast diodes (t_{RR} of 35 ns or lower is recommended) due to the MCM operation and high ambient temperature requirement. Diodes with high blocking voltage and low t_{RR} are uncommon and thus two diodes in series were implemented in order to meet 70% repetitive peak reverse voltage derating for the diodes. Capacitor C5 was selected to meet the output voltage ripple requirement. Other considerations for the selection include a minimum capacitor expected life of 40,000 hours and adequate capacitor ripple current rating. Capacitor C6 provides further filtering of high frequency output voltage ripple.

4.4 Output Feedback

During the IC1 off-time, capacitor C4 is charged to the output voltage via diode D3. This voltage is used to provide feedback to the IC via the resistor divider formed by resistors R1 and R2. The FEEDBACK (FB) pin is sampled by the controller during each switching cycle. A current greater than 49 μA into the FB pin will inhibit the switching of the internal power MOSFET while a current below will allow switching cycles to occur.

Due to the high difference between the input voltage and output voltage, the IC1 on-time becomes very low. Since the operation is on-off and highly dependent on the voltage on C4, the feedback response can be very aggressive resulting to pulse bunching and higher output ripple. To mitigate this, a resistor, R4, is placed in series with C4. Resistor R4 lessens feedback sensitivity and stabilizes the control loop resulting in a more even spread of switching pulses.

5 PCB Layout

Layers:	Four (4)
Board Material:	FR4
Board Thickness:	1.6 mm
Copper Weight:	1 oz. (All layer)

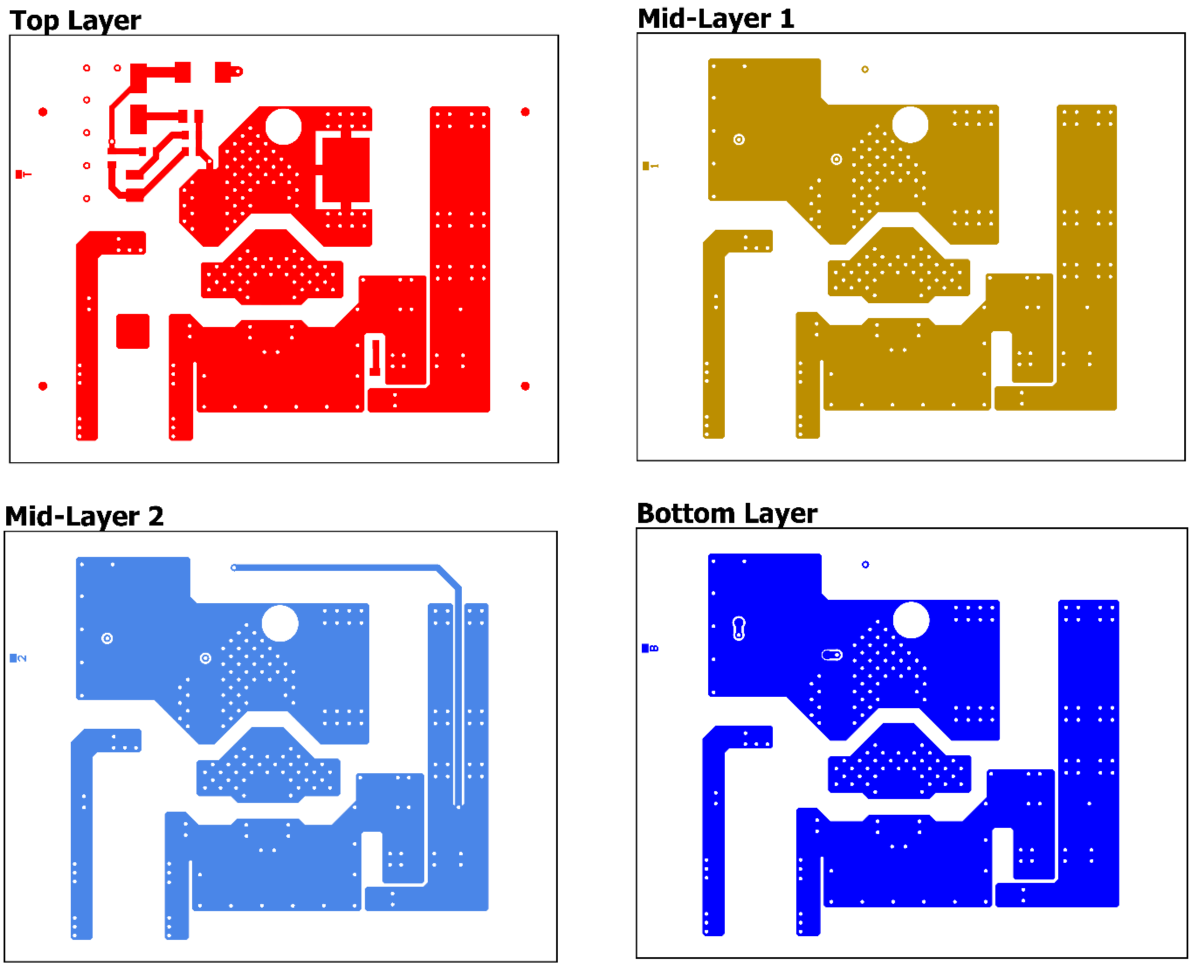


Figure 5 – DER-965Q PCB Layout.

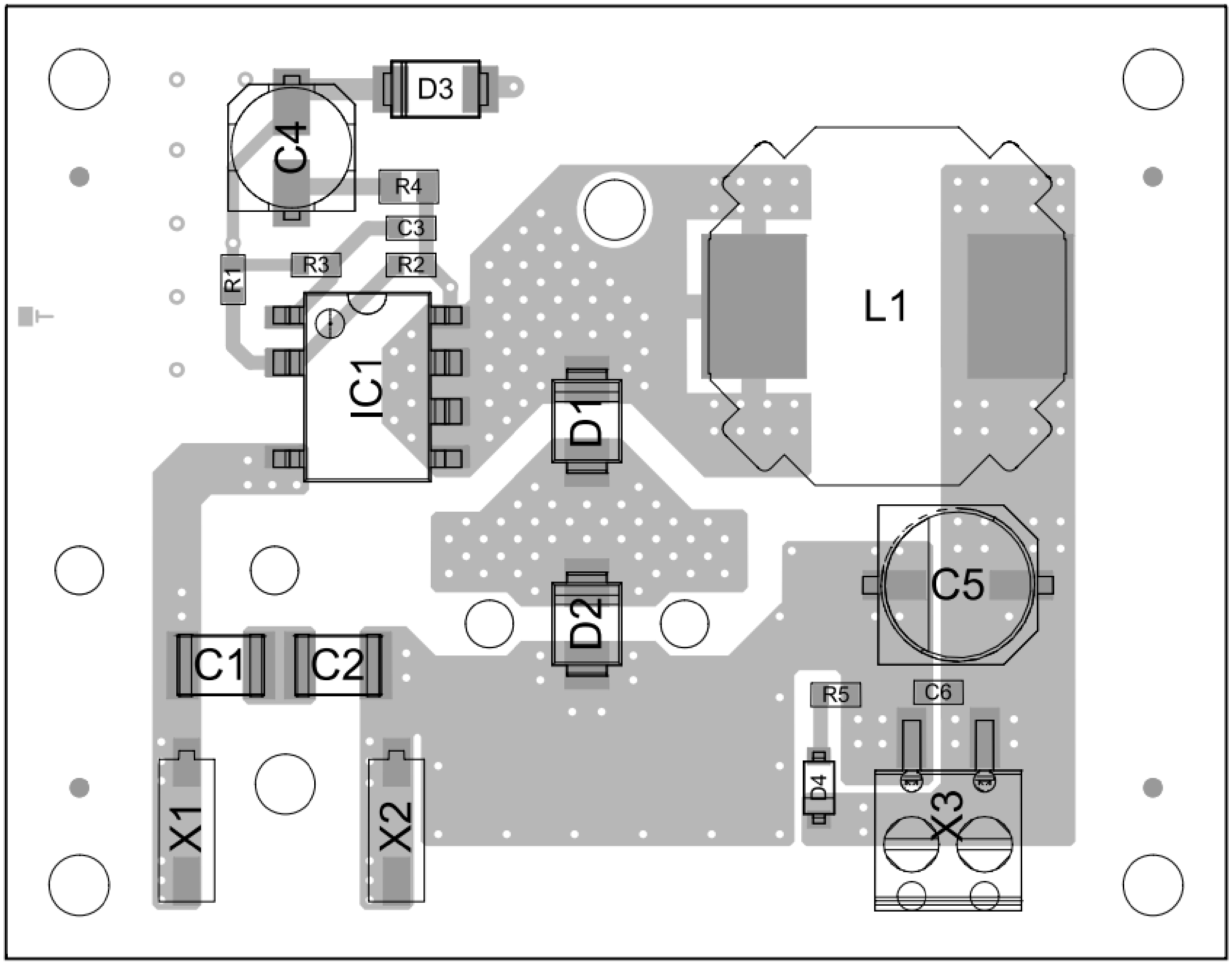


Figure 6 – DER-965Q PCB Assembly.

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	2	C1, C2	Multilayer Ceramic Capacitors MLCC - SMD/SMT 630 V 100 nF X7R 1812 10% AEC-Q200	GCJ43DR72J104KXJ1L	Murata
2	2	C3, C6	Multilayer Ceramic Capacitors MLCC - SMD/SMT 50 V 100 nF X7R 0603 10% AEC-Q200	CL10B104KB8WPNC	Samsung
3	1	C4	Polymer Aluminum Capacitors – 50 V 22 μF 20% AEC-Q200	HHXC500ARA220MF61G	United Chemi-Con
4	1	C5	Polymer Aluminum Capacitors – 25 V 220 μF 20% AEC-Q200	25PSV220M8X10.5	Rubycon
5	2	D1, D2	Diode Ultra-Fast Recovery 600 V 3 A SMT DO-214AA (SMB) AEC-Q101	ES3JBHR5G	Taiwan Semi
6	1	D3	Diode Fast Recovery 1 kV 1 A SMT DO-214AC (SMA) AEC-Q101	ACURA107-HF	Comchip
7	1	D4	Zener Diode 17 V 500 mW ±2% SMT SOD-123 AEC-Q101	MMSZ5247C-HE3-08	Vishay
8	1	IC1	LinkSwitch-TN2Q, SMD-8C, AEC-Q100	LNK3209GQ	Power Integrations
9	1	L1	Shielded Power Inductor – 330 μH 1.68 A MSS1812T AEC-Q200	MSS1812T-334KED	Coilcraft
10	1	R1	Thick Film Resistors - SMD 16.9 kΩ 0.1 W 0603 1% AEC-Q200	ERJ-3EKF1692V	Panasonic
11	1	R2	Thick Film Resistors - SMD 2.49 kΩ 0.1 W 0603 1% AEC-Q200	ERJ-3EKF2491V	Panasonic
12	1	R3	Thick Film Resistors - SMD 36 kΩ 0.1 W 0603 1% AEC-Q200	RMCF0603FT36K0	Stackpole
13	1	R4	Thick Film Resistors - SMD 15 Ω 0.125 W 0805 5% AEC-Q200	CRCW080515R0JNEA	Vishay
14	1	R5	Thick Film Resistors - SMD 160 Ω 0.1 W 0603 1% AEC-Q200	ERJ-3EKF1600V	Panasonic
15	1	X1	PCB Terminal Block – SMD 0.5 mm white	2059-301/998-403	WAGO Corporation
16	1	X2	PCB Terminal Block – SMD 0.5 mm black	2059-321/998-403	WAGO Corporation
17	1	X3	PCB Terminal Block – 1x2 pin 3.81 mm pitch	2383945-2	TE

Table 4 – DER-965Q Bill of Materials.

7 Assembly Notes

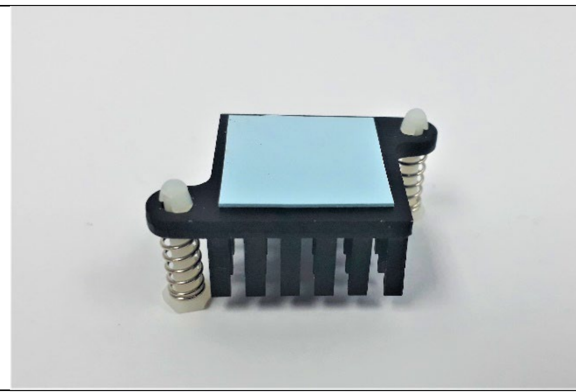
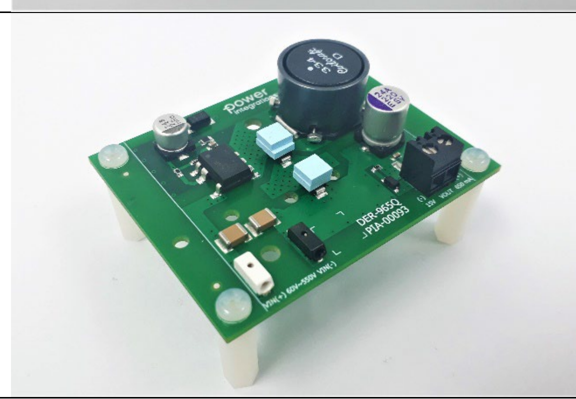
7.1 *Heat Sink Assembly*

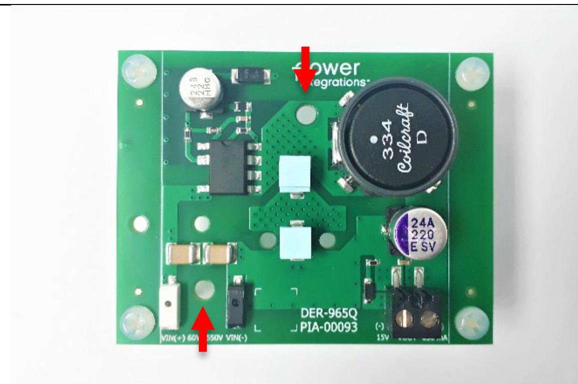
7.1.1 Material List

Item	Description	Qty	Part Number	Manufacturer
[1]	Heat Sink: BGA Aluminum Top Mount 23x12 mm Front Push Pin	1	960-23-12-F-AB-0	Wakefield-Vette
[2]	Thermal Pad: A6200 20x20x0.5 mm	1	TG-A6200-20-20-0.5	t-Global Technology
[3]	Thermal Pad: A6200 5x5x1.5 mm	4	TG-A6200-5-5-1.5	t-Global Technology

Table 5 – Heat Sink Assembly Material List.

7.1.2 Heat Sink Assembly Instructions

Carefully place one piece of Item [2] on the bottom side of the heat sink, Item [1]. Gently flatten it on the surface of the heat sink to ensure that it sticks. Use any appropriate tool. Do not use bare hands.	
Using any appropriate tool, put 2 pieces of Item [3], vertically stacked, on top of both the freewheeling diodes D1 and D2.	

With the heat sink oriented for top mounting, carefully align the heat sink's push pins on top of the two holes indicated in the picture. Slowly lower the heat sink until it touches the thermal pads (Item [3]) on top of the diodes.	
Push one pin towards the hole while applying appropriate pressure on the opposite side of the heat sink. When the pin is secured, push the 2nd pin while still applying pressure on the same side. Lastly, check if the heat sink coupled correctly with the IC1 and the thermal pads on D1 and D2.	

8 Design Spreadsheet

8.1 PI Expert Online

PI Expert Online (https://www.power.com/design-support/pi-expert) is a web-based program that takes specifications and automatically generates a power conversion solution. Table 6 shows the generated design spreadsheet from PI Expert Online where the design was based on.

1	**DCDC_LinkSwitchTN2-Automotive-Buck_082422; Rev.2.1; Copyright Power Integrations 2022**	**INPUT**	**OUTPUT**	**UNIT**	**DCDC LinkSwitchTN2-Automotive Buck Converter**
2	**APPLICATION VARIABLES**				
3	VDCMIN	60.00	60.00	V	Minimum DC voltage
4	VDCMAX	550.00	550.00	V	Maximum DC input voltage
5	VOUT	15.00	15.00	V	Output voltage
6	IOUT	0.650	0.650	A	Average output current
7	EFFICIENCY_ESTIMATED		0.80		Efficiency estimate at output terminals
8	EFFICIENCY_CALCULATED		0.77		Calculated efficiency based on real components and operating point
9	POUT		9.75	W	Continuous output power
10	INPUT STAGE RESISTANCE		10	Ohms	Input stage resistance in ohms (includes thermistor, filtering components, etc)
11	PLOSS_INPUTSTAGE		0.413	W	Maximum input stage loss
15	**CONTROLLER VARIABLES**				
16	OPERATION MODE		MCM		Mostly continuous mode of operation
17	CURRENT LIMIT MODE	STD	STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
18	PACKAGE		SMD-8C		Select the device package
19	DEVICE SERIES	AUTO	LNK3209		Generic LinkSwitch-TN2 device
20	DEVICE CODE		LNK3209GQ		Required LinkSwitch-TN2 device
21	ILIMITMIN		1.079	A	Minimum current limit of the device
22	ILIMITTYP		1.300	A	Typical current limit of the device
23	ILIMITMAX		1.521	A	Maximum current limit of the device
24	RDSON		4.37	ohms	Primary switch on-time drain to source resistance at 125degC
25	FSMIN		62000	Hz	Minimum switching frequency
26	FSTYP		66000	Hz	Typical switching frequency
27	FSMAX		70000	Hz	Maximum switching frequency
28	BVDSS		750	V	Device breakdown voltage
32	**PRIMARY SWITCH PARAMETERS**				
33	VDSON		2.00	V	Primary switch on-time drain to source voltage estimate
34	VDSOFF		578	V	Primary switch off-time drain-to-source voltage stress
35	DUTY		0.290		Maximum duty cycle
36	TIME_ON_MIN		0.872	us	Primary switch minimum on-time
37	IPED_PRIMARYSWITCH		0.235	A	Maximum primary switch pedestal current
38	IRMS_PRIMARYSWITCH		0.436	A	Maximum primary switch RMS current
39	PLOSS_PRIMARYSWITCH		0.895	W	Maximum primary switch loss
43	**BUCK INDUCTOR PARAMETERS**				
44	INDUCTANCE_MIN		297	uH	Minimum design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant
45	INDUCTANCE_TYP	330	330	uH	Typical design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant

46	INDUCTANCE_MAX		363	uH	Maximum design inductance required for current delivery. Note that the chosen inductor must be AEC-Q200 compliant
47	TOLERANCE_INDUCTANCE		10	%	Tolerance of the design inductance
48	DC RESISTANCE OF INDUCTOR	0.3	0.3	ohms	DC resistance of the buck inductor
49	FACTOR_KLOSS		0.50		Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%)
50	IRMS_INDUCTOR		0.978	A	Maximum inductor RMS current
51	PLOSS_INDUCTOR		0.287	W	Maximum inductor losses
55	**FREEWHEELING DIODE PARAMETERS**				
56	VF_FREEWHEELING		2.60	V	Forward voltage drop across the two freewheeling diodes in series
57	PIV_RATING		600.00	V	Peak inverse voltage rating of each freewheeling diode
58	TRR		35	ns	Reverse recovery time of each freewheeling diode
59	PIV_CALCULATED		578	V	Computed peak inverse voltage across the freewheeling diodes
60	IRMS_DIODE		0.962	A	Maximum diode RMS current
61	PLOSS_DIODE		1.896	W	Maximum loss across both freewheeling diodes
62	RECOMMENDED DIODE	ES1J[3]	ES1J		Recommended freewheeling diode. Two of this diode in series must be implemented to pass 80% voltage derating and thermal requirements
66	**BIAS/FEEDBACK PARAMETERS**				
67	VF_BIAS		0.70	V	Forward voltage drop of the bias diode
68	RBIAS		2490	Ohms	Bias resistor
69	CBP		0.1	uF	BP pin capacitor
70	RFB		17400	Ohms	Feedback resistor
71	CFB		10	uF	Feedback capacitor
72	C_SOFTSTART		1-10	uF	If the output voltage is greater than 12 V or total output and system capacitance is greater than 100 uF, a soft start capacitor between 1uF and 10 uF is recommended
73	PLOSS_FEEDBACK		0.011	W	Maximum feedback component losses
77	**OUTPUT CAPACITOR**				
78	OUTPUT VOLTAGE RIPPLE	240	240	mV	Desired output voltage ripple
79	IRMS_COUT		0.730	A	Maximum output capacitor RMS current
80	PLOSS_COUT		0.012	W	Maximum output capacitor power loss
81	ESR_COUT	22	22	mOhms	ESR of the output capacitor

Table 6 – DER-965Q PI Expert Online Spreadsheet.

[3] Freewheeling diode used for the design has similar relevant parameters as the recommended diode.

9 Performance data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a High Voltage (HV) room.

Figure 7 – High Voltage Test Set-up.

Figure 8 – Test Set-up Inside the High Voltage Room.

2. Unit under test was placed under a box while inside the thermal chamber to eliminate the effect of any airflow.

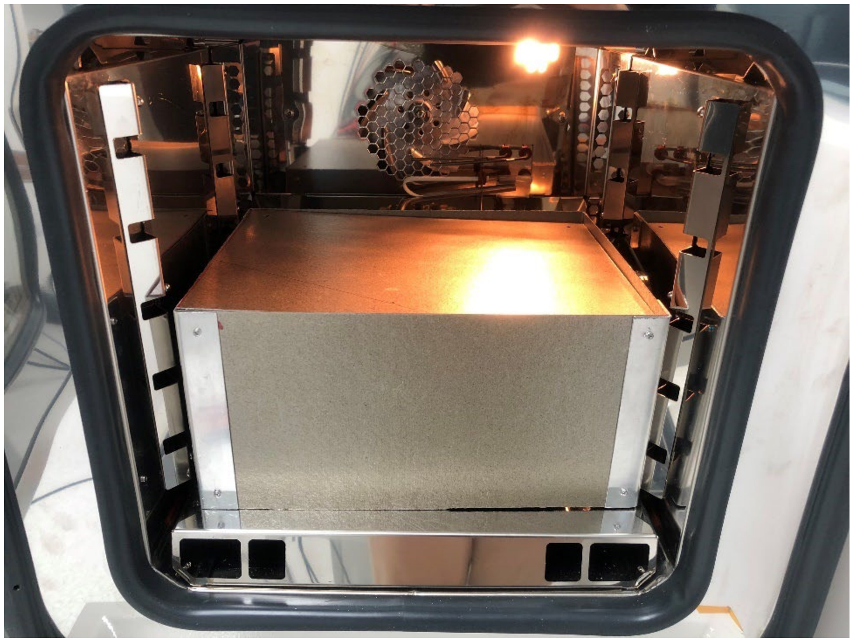


Figure 9 - Unit under test placed under a box to eliminate the effect of airflow.

3. For data points showing performance across varying input line voltages and output load currents, the unit under test was soaked at full load condition for at least 5 min. for every change in the input voltage during the start of every test sequence. Also, for every loading condition, the unit under test was soaked for at least 20 s before measurements were taken.

9.1 Efficiency

9.1.1 Line Efficiency[4]

Line efficiency describes how the change in input voltage affects the overall efficiency of the unit.

Sudden increase of efficiency recorded at 550 V_{DC} input and 105 °C ambient temperature is due to a change of operation mode of the LNK3209GQ device and output power deration at 550 VDC, 105 °C ambient temperature.

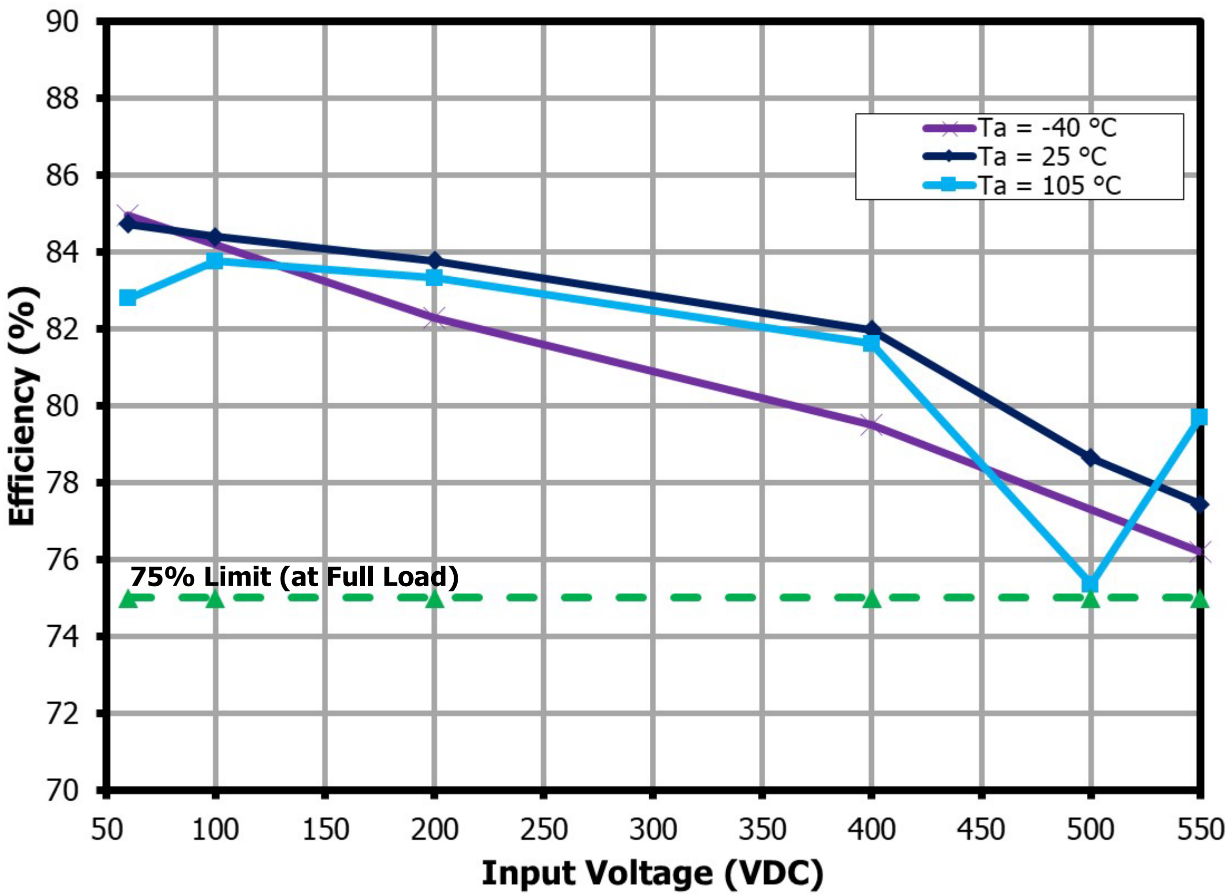


Figure 10 – Full Load Efficiency vs. Input Line Voltage.

[4] Power is derated to 8.25 W at 550 V_{DC} input, 105 °C ambient temperature.

9.1.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the overall efficiency of the unit.

9.1.2.1 Efficiency vs. Load at 105 °C Ambient[5]

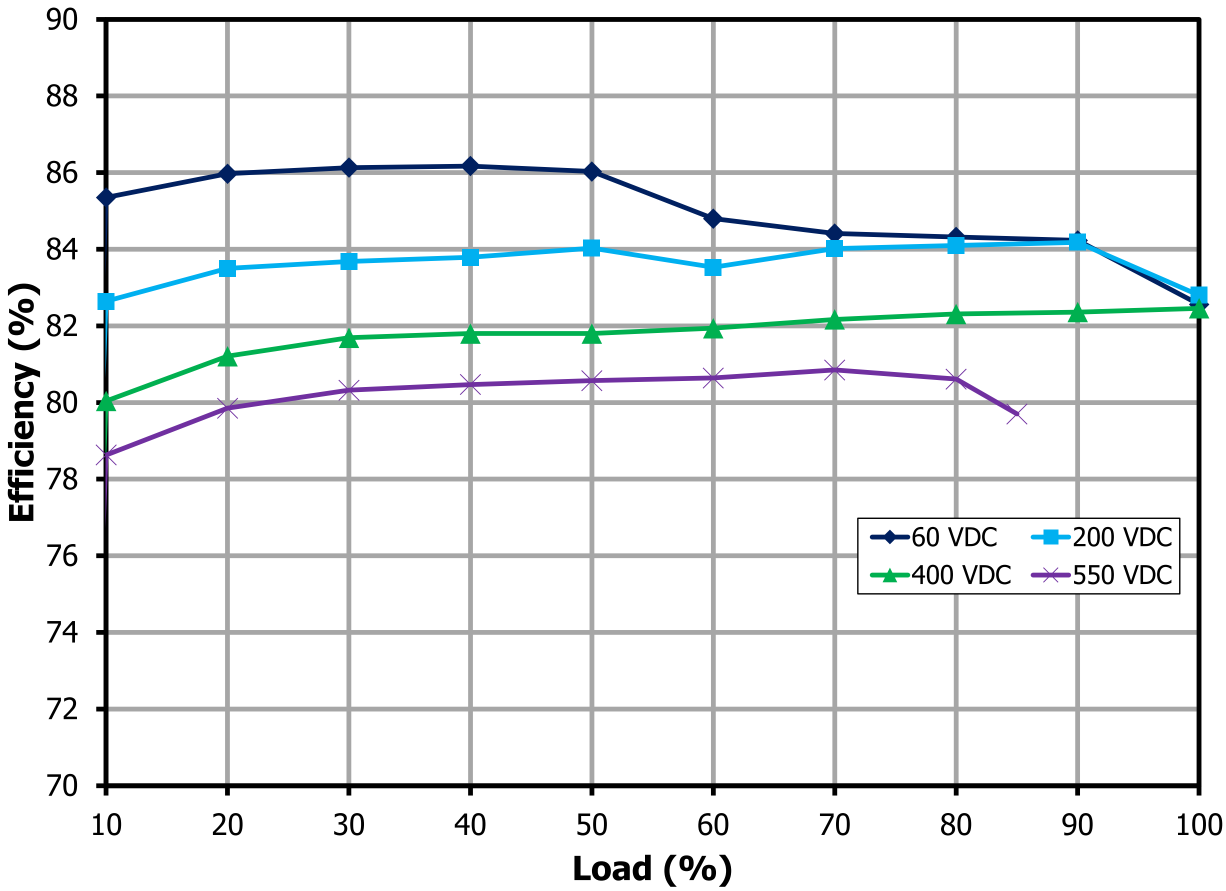


Figure 11 – Efficiency vs. Load at Different Input Voltages (105 °C Ambient).

[5] Power is derated to 8.25 W at 550 V_{DC} input, 105 °C ambient temperature.

9.1.2.2 Efficiency vs. Load at 25 °C Ambient

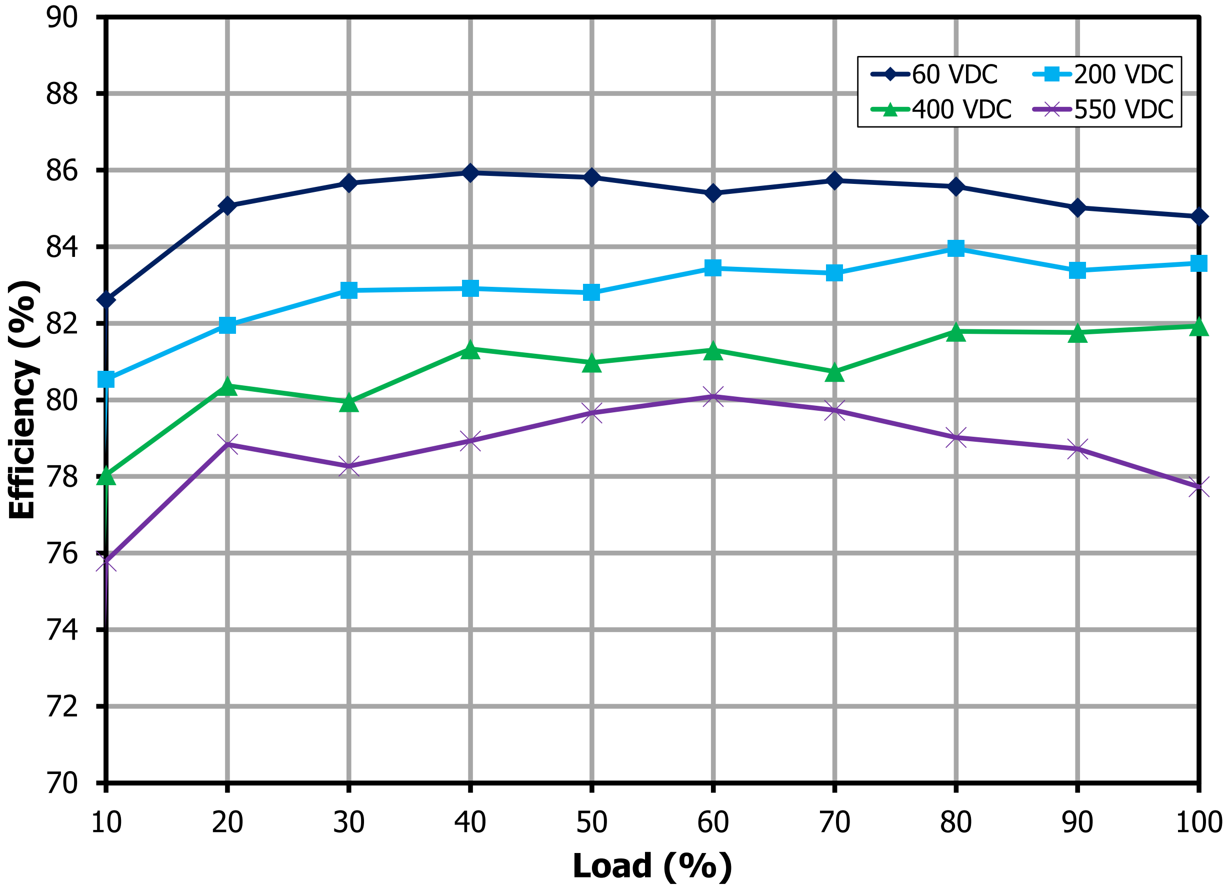


Figure 12 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.1.2.3 Efficiency vs. Load at -40 °C Ambient

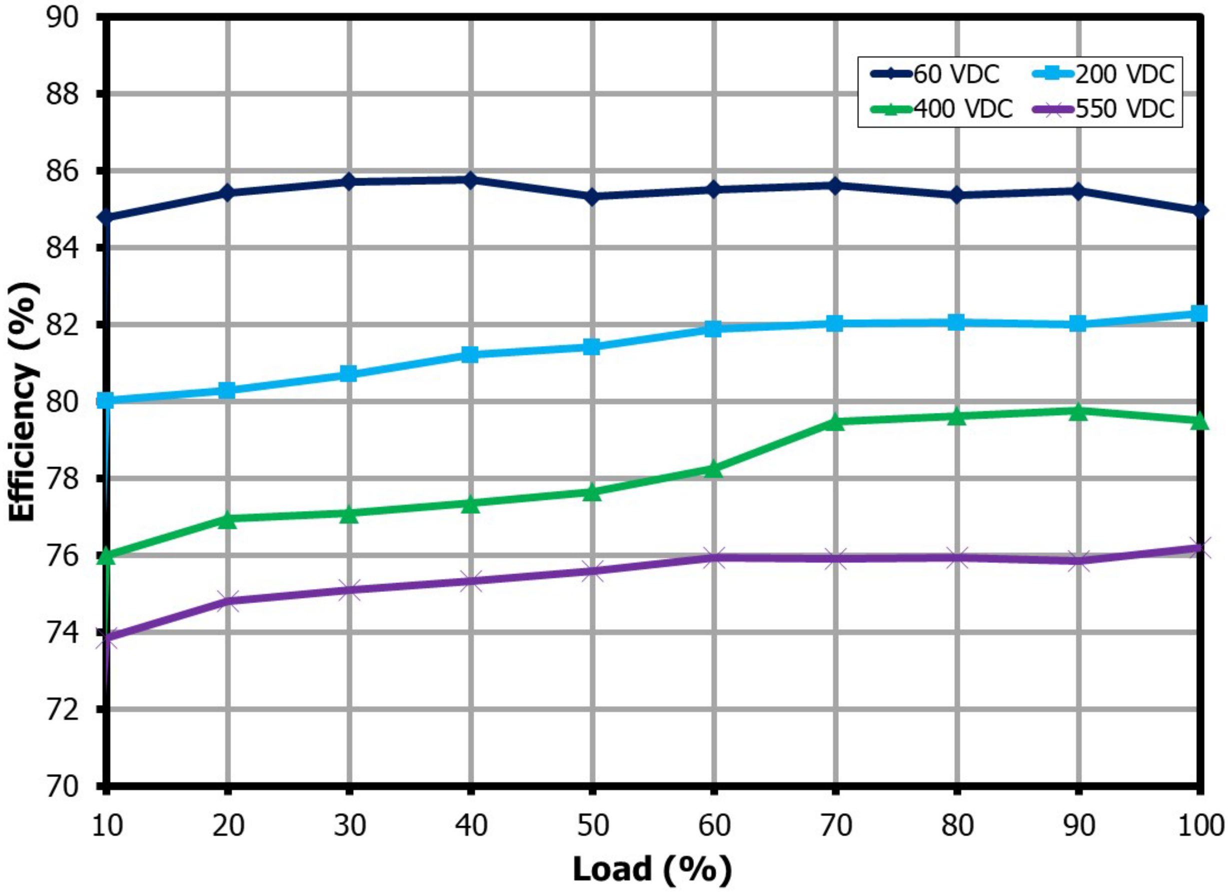


Figure 13 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.2 Output Line and Load Regulation at 105 °C Ambient

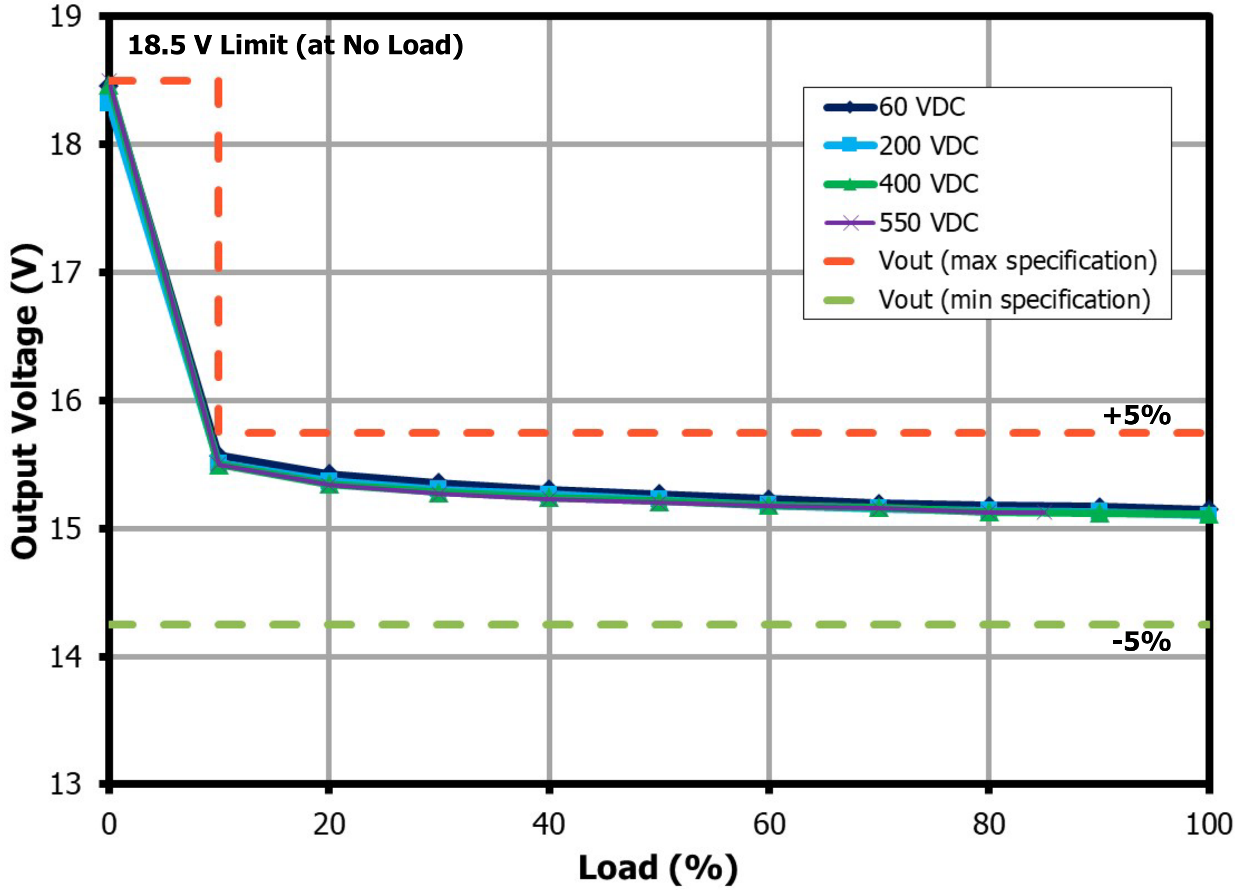


Figure 14 – Output Regulation vs. Load at Different Input Voltages (105 °C Ambient).

9.3 Output Line and Load Regulation at 25 °C Ambient

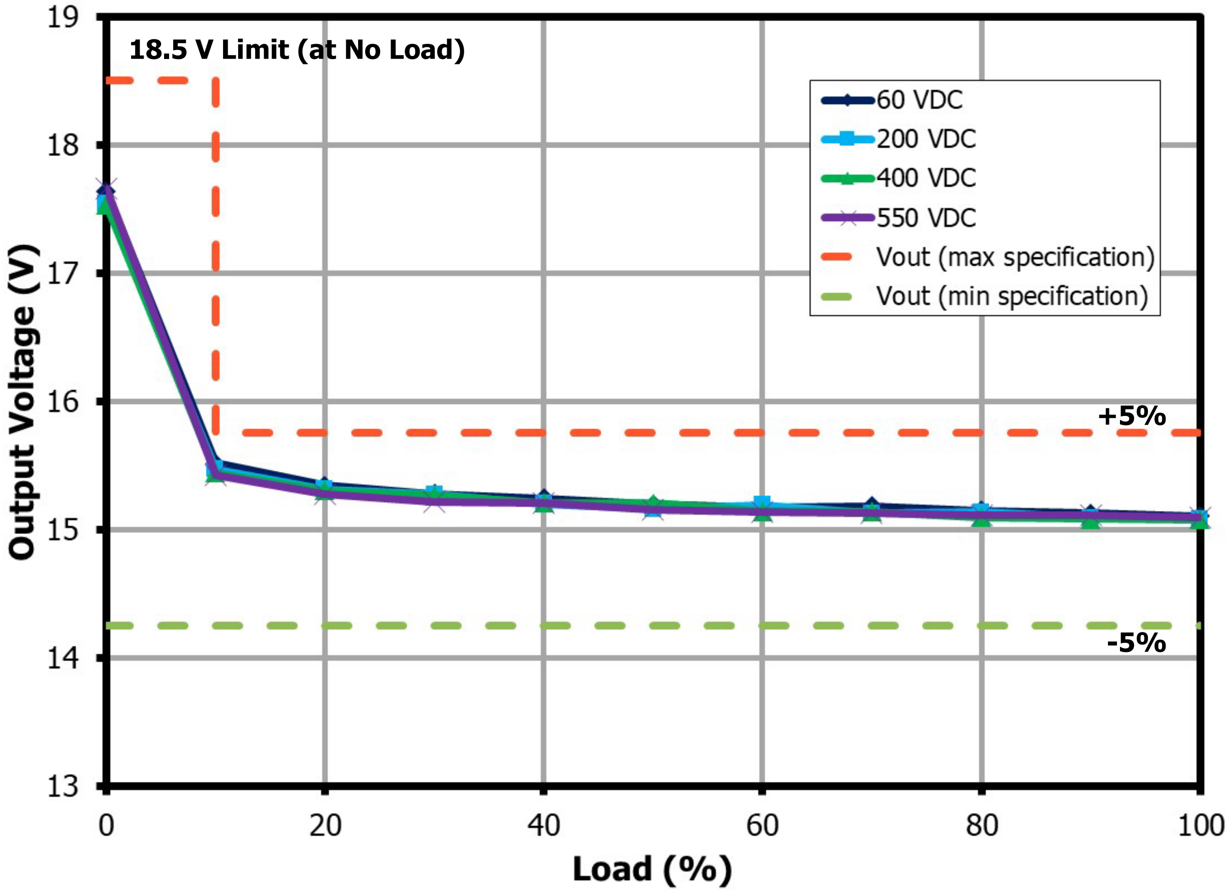


Figure 15 – Output Regulation vs. Load vs. Line Voltage (25 °C Ambient).

9.4 Output Line and Load Regulation at -40 °C Ambient

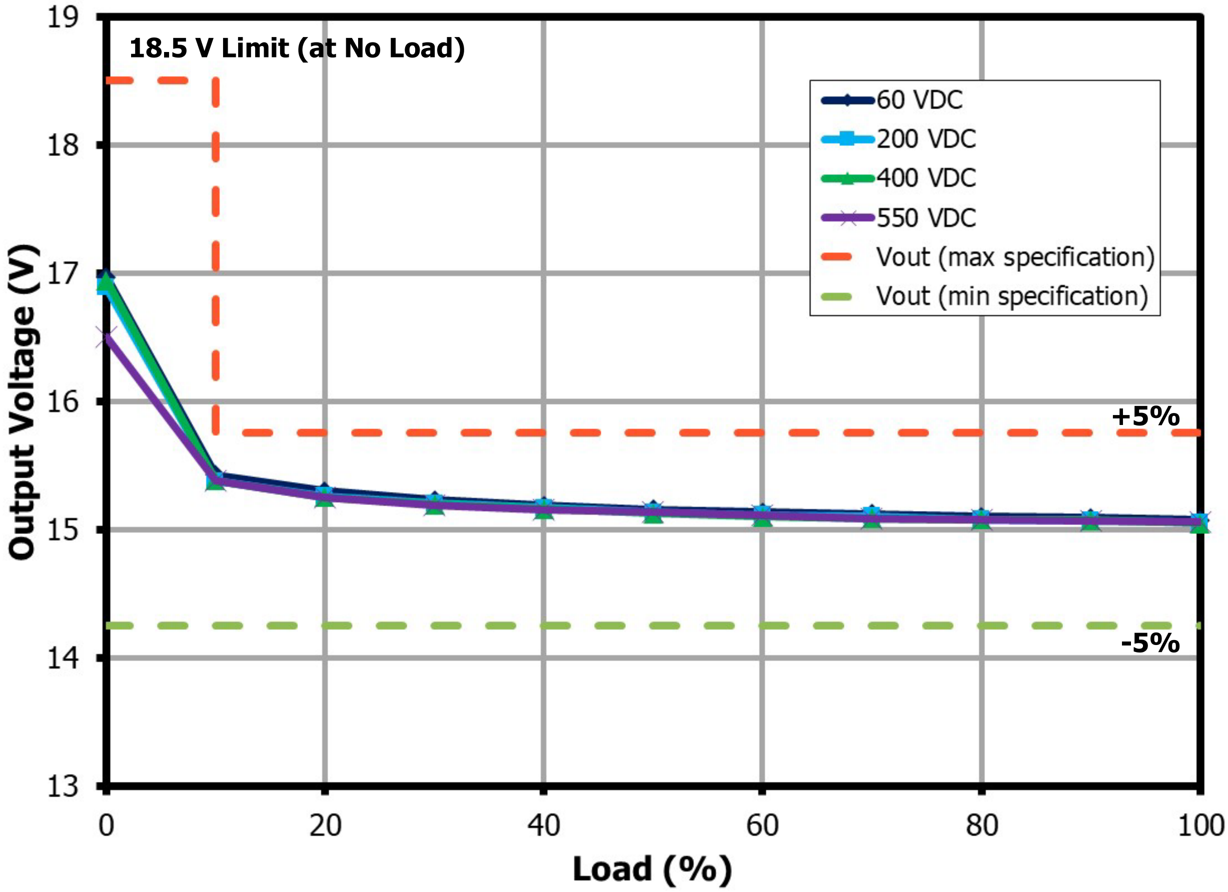


Figure 16 – Output Regulation vs. Load vs. Line Voltage (-40 °C Ambient).

10 Thermal Performance

10.1 Thermal Data at 105 °C Ambient Temperature

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 9 shows the set-up for thermal measurement. The unit was tested with the heat sink assembled.

Critical components	Input Voltage		
	60 V_{DC}	400 V_{DC}	550 V_{DC}[6]
LinkSwitch-TN2Q (IC1)	130.9	126.9	131.2
Freewheeling Diode 1 (D1)	127.8	128.3	130.6
Freewheeling Diode 2 (D2)	125.2	126.4	128.1
Output Inductor (L1)	119.9	127.6	129.6
Ambient Temperature	105	104.9	105.1

Table 7 – Thermals Data at 105 °C at Different Input Voltages.

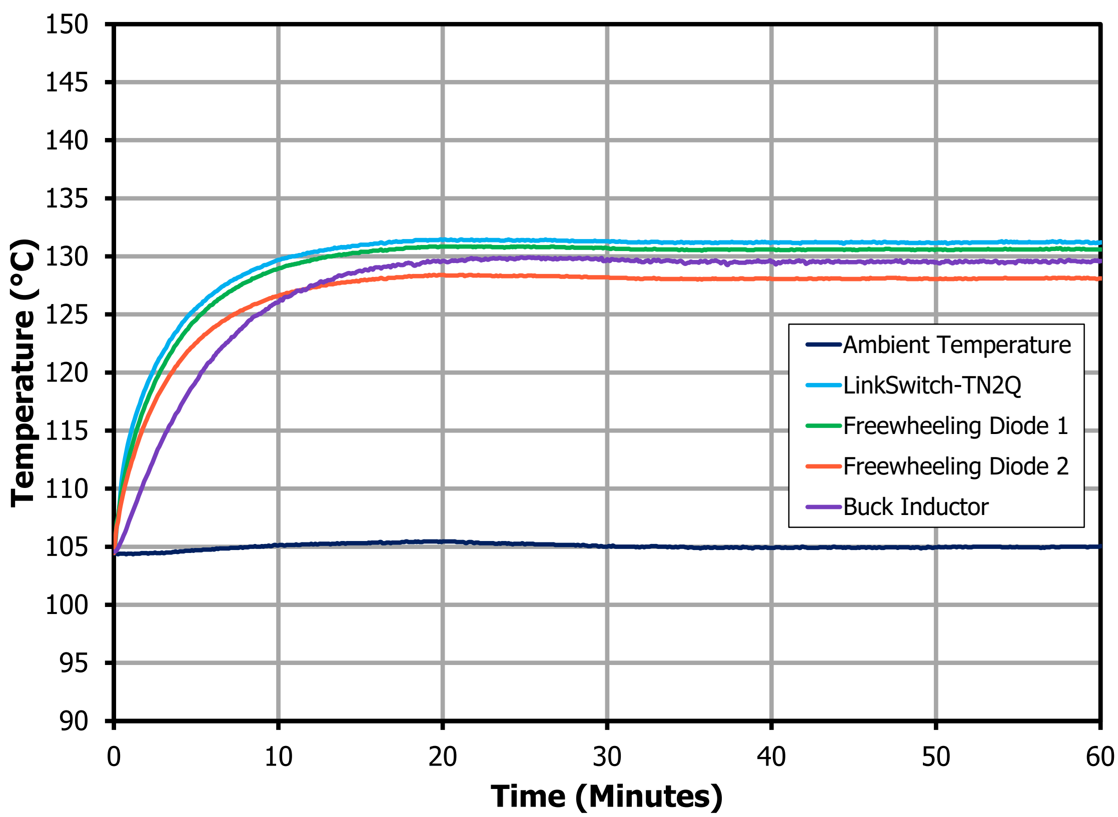


Figure 17 – Component Temperatures at 105 °C Ambient, 550 V_{DC} Input, Output Derated to 550 mA (8.25 W).

[6] Power is derated to 8.25 W at 550 V_{DC} input, 105 °C ambient temperature.

10.2 Thermals Data at 25 ºC Ambient Temperature

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour in an enclosure to minimize the effect of air flow. The unit was tested without the heat sink to capture component temperatures via the Fluke thermal imager.

This indicates the design can deliver full power at an ambient of up to 50 ºC without the heatsink – with an estimated maximum temperature of for IC1 of 110 ºC.

In a final implementation in an automotive subsystem, it is expected that the heatsink is replaced by contact between the thermal pads and the outer enclosure wall.

Critical components	Input Voltage		
	60 V_{DC}	400 V_{DC}	550 V_{DC}
LinkSwitch-TN2Q (IC1)	63.0	60.8	85.7
Freewheeling Diode 1 (D1)	62.0	70.3	81.9
Freewheeling Diode 2 (D2)	57.2	66.4	73.4
Output Inductor (L1)	49.2	58	67.6
Ambient Temperature	24.5	24.4	26.0

Table 8 – Thermals Data at 25 °C at Different Input Voltages.

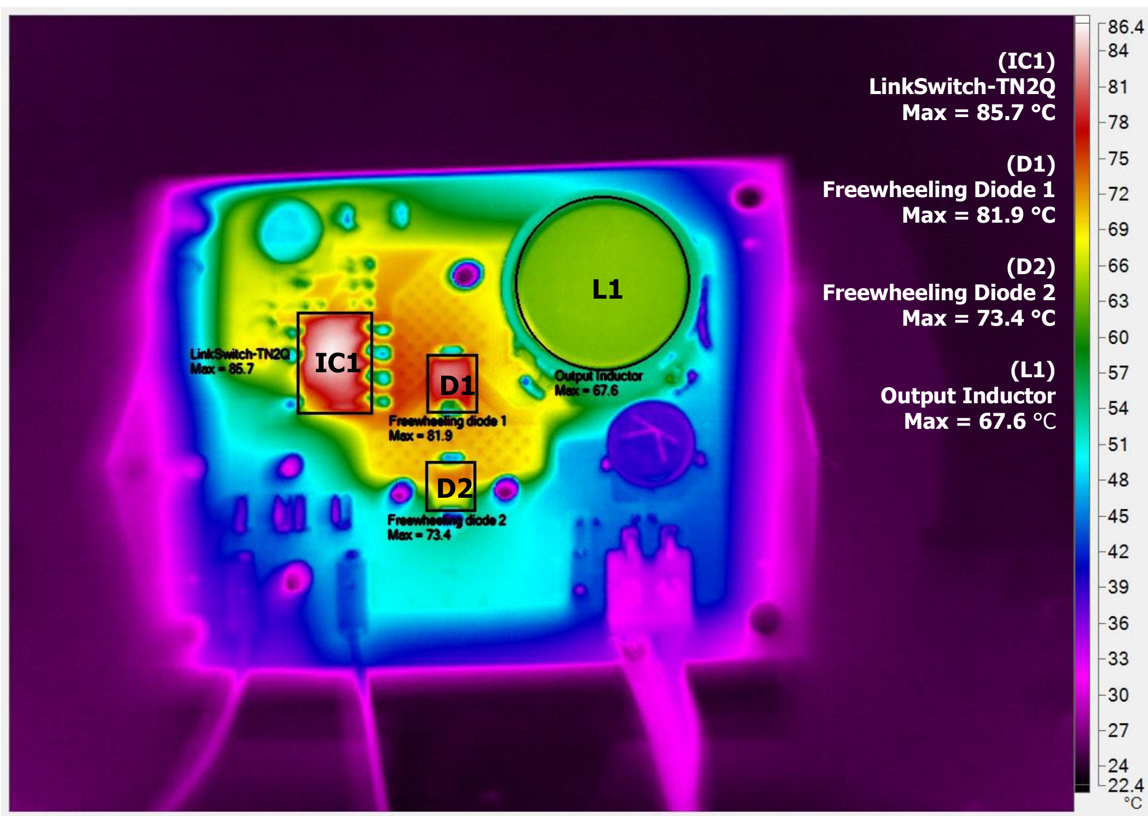


Figure 18 – Top PCB Thermal Scans at 550 V_{DC} Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by hot plugging-in the unit under test to a DC link capacitor fully charged[7] to a test input voltage of HV+.

11.1.1 Output Voltage and Current at 25 °C Ambient Temperature[8]

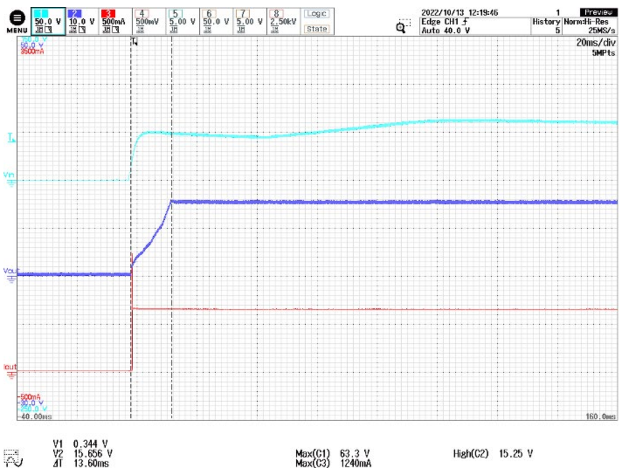


Figure 19 – Output Voltage and Current.
60 V_{DC}, 650 mA Load
CH1: V_{IN}, 50 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

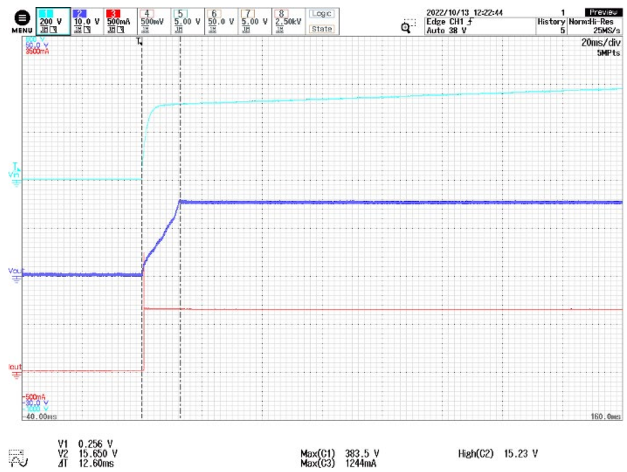


Figure 20 – Output Voltage and Current.
400 V_{DC}, 650 mA Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

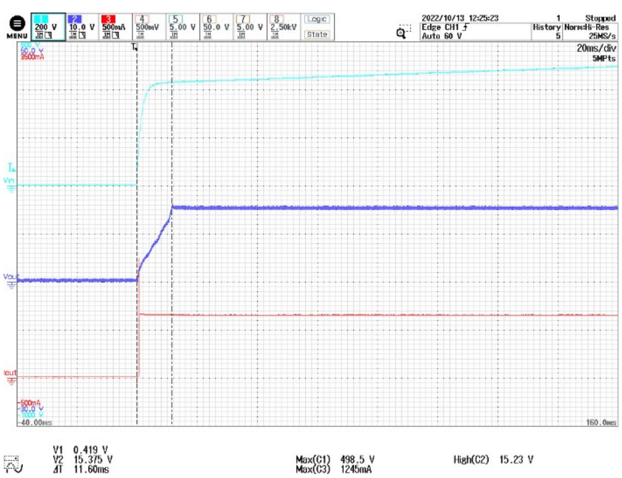


Figure 21 – Output Voltage and Current.
550 V_{DC}, 650 mA Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

[7] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[8] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.

11.1.2 LinkSwitch-TN2Q Drain Voltage and Current at 25 ºC Ambient Temperature

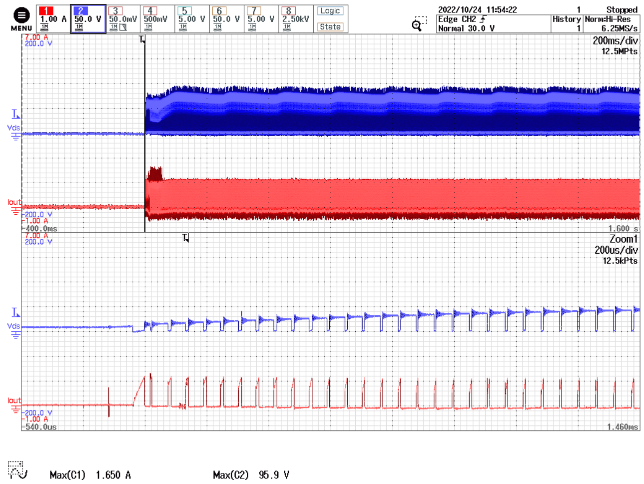


Figure 22 – LNK3209GQ Drain Voltage and Current.
60 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 50 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

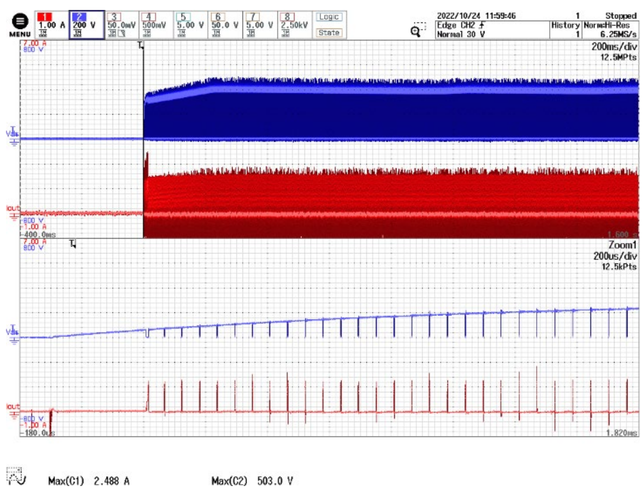


Figure 23 – LNK3209GQ Drain Voltage and Current.
400 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

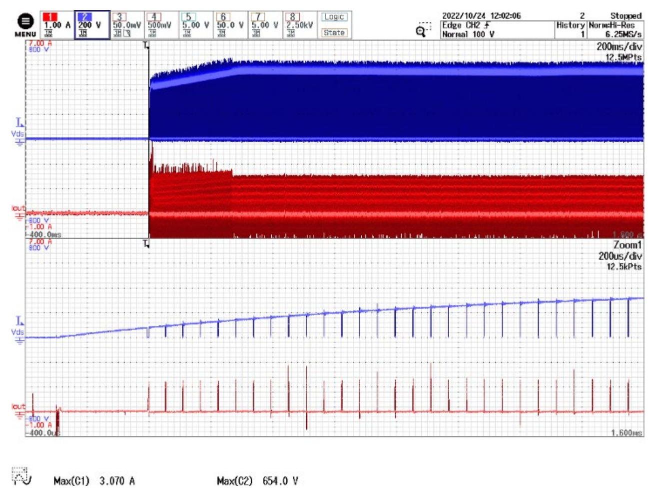


Figure 24 – LNK3209GQ Drain Voltage and Current.
550 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

11.1.3 Freewheeling Diode Voltages at 25 °C Ambient Temperature

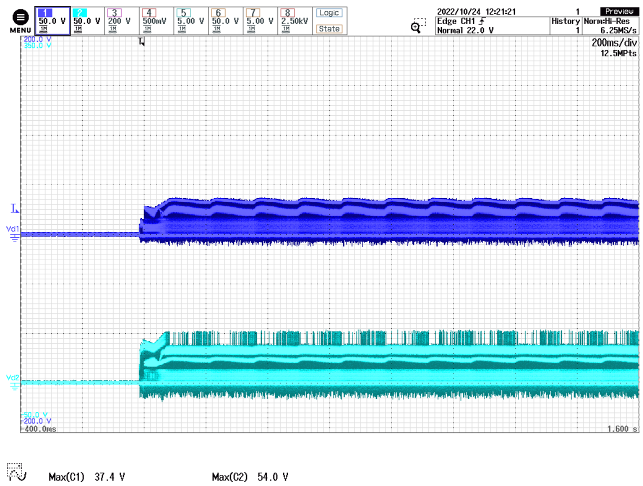


Figure 25 – Freewheeling Diode Voltages.
60 V_{DC}, 650 mA Load.
CH1: V_{D1}, 50 V / div.
CH2: V_{D2}, 50 V / div.
Time: 200 ms / div.

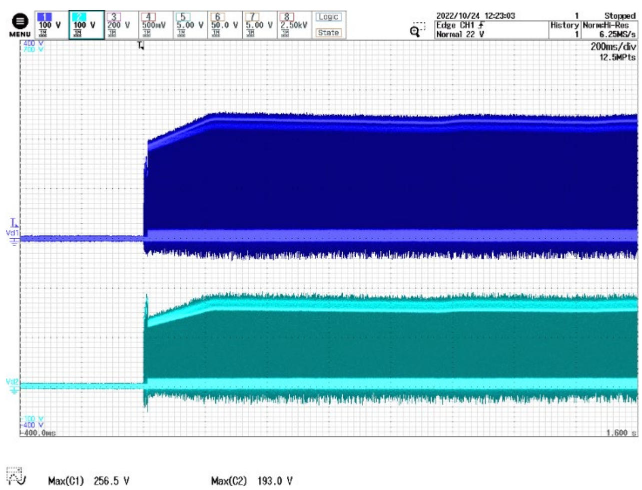


Figure 26 – Freewheeling Diode Voltages.
400 V_{DC}, 650 mA Load.
CH1: V_{D1}, 100 V / div.
CH2: V_{D2}, 100 V / div.
Time: 200 ms / div.

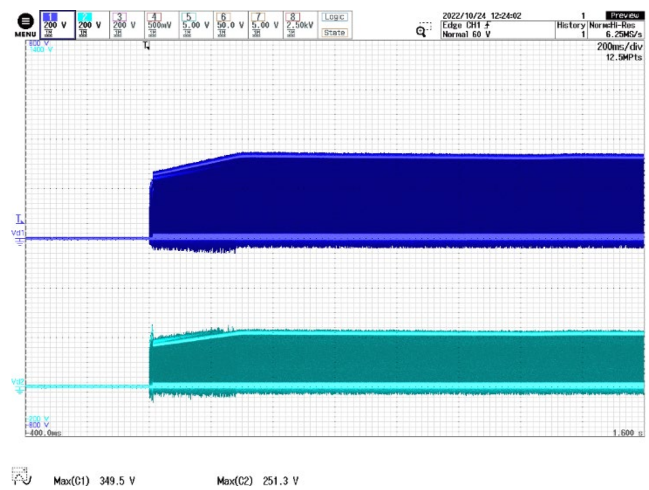


Figure 27 – Freewheeling Diode Voltages.
550 V_{DC}, 650 mA Load.
CH1: V_{D1}, 200 V / div.
CH2: V_{D2}, 200 V / div.
Time: 200 ms / div.

11.1.4 Output Voltage and Current at -40 °C Ambient Temperature[9]

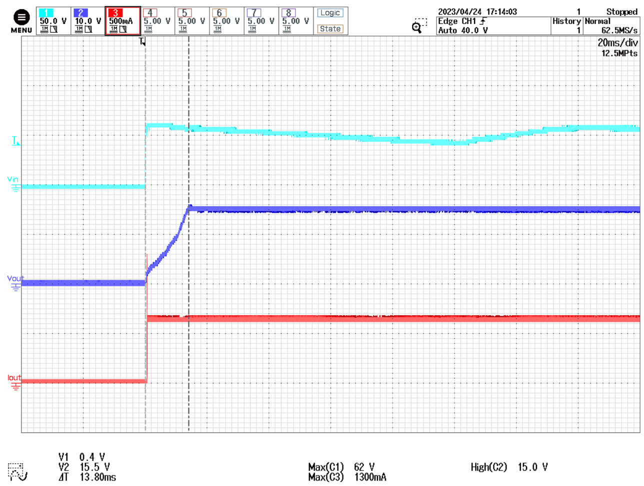


Figure 28 – Output Voltage and Current.
60 V_{DC}, 650 mA Load
CH1: V_{IN}, 50 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

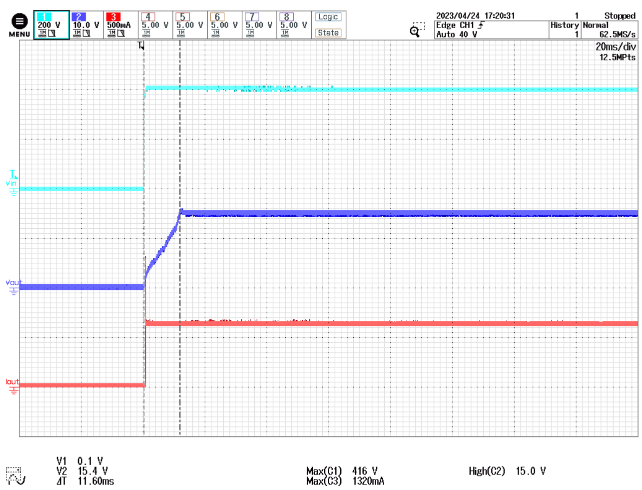


Figure 29 – Output Voltage and Current.
400 V_{DC}, 650 mA Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

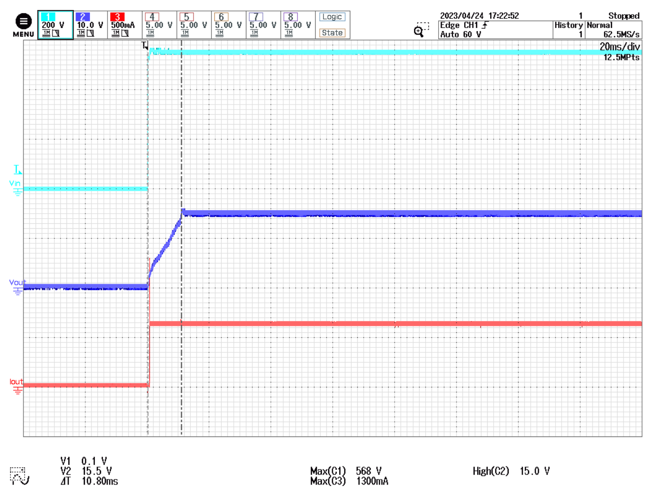


Figure 30 – Output Voltage and Current.
550 V_{DC}, 650 mA Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 500 mA / div.
Time: 20 ms / div.

[9] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.

11.1.5 LinkSwitch-TN2Q Drain Voltage and Current at -40 ºC Ambient Temperature

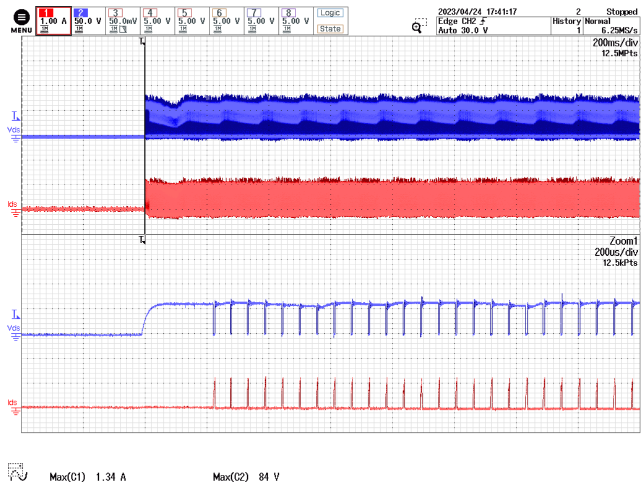


Figure 31 – LNK3209GQ Drain Voltage and Current.
60 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 50 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

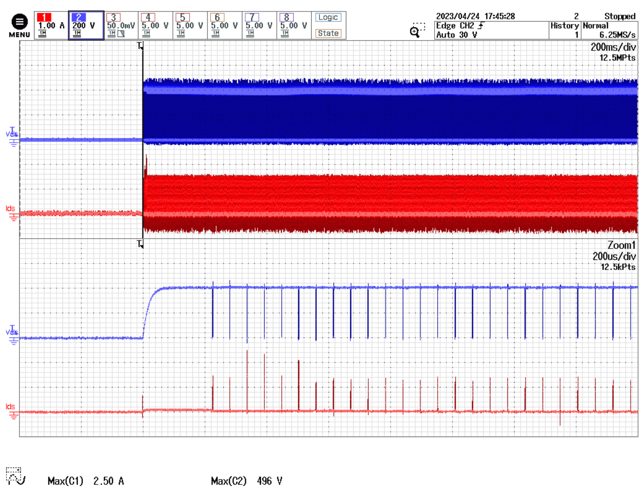


Figure 32 – LNK3209GQ Drain Voltage and Current.
400 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

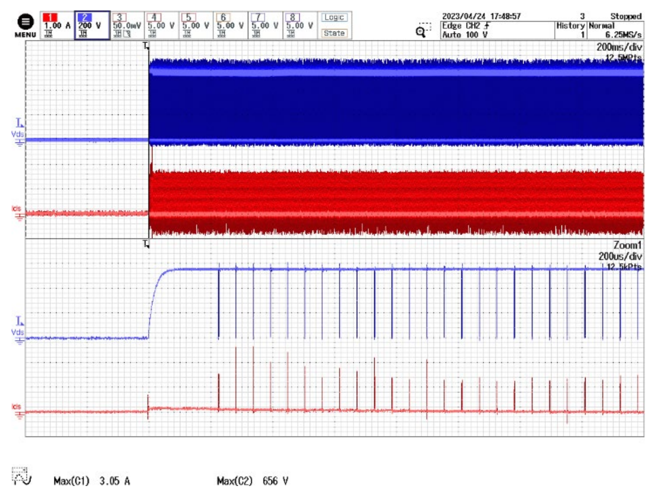


Figure 33 – LNK3209GQ Drain Voltage and Current.
550 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 200 ms / div.
Zoom: 200 µs / div.

11.1.6 Freewheeling Diode Voltages at -40 °C Ambient Temperature

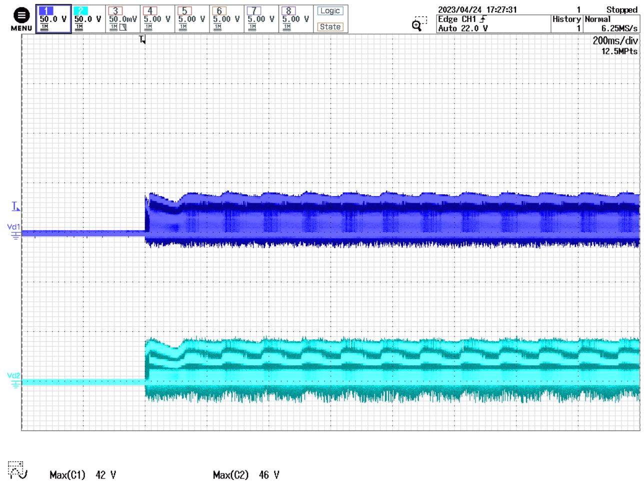


Figure 34 – Freewheeling Diode Voltages.
60 V_{DC}, 650 mA Load.
CH1: V_{D1}, 50 V / div.
CH2: V_{D2}, 50 V / div.
Time: 200 ms / div.

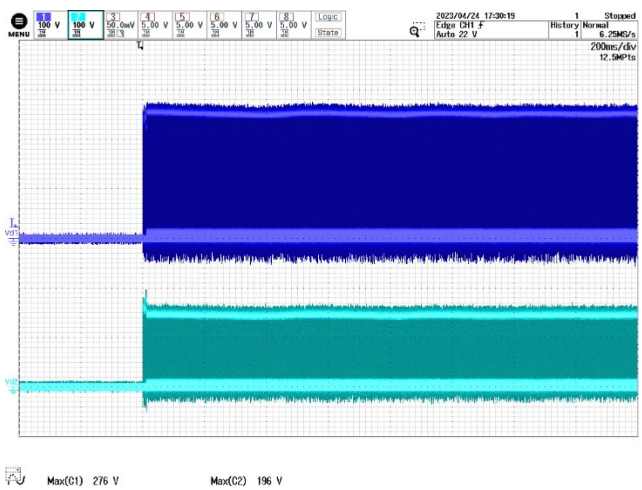


Figure 35 – Freewheeling Diode Voltages.
400 V_{DC}, 650 mA Load.
CH1: V_{D1}, 100 V / div.
CH2: V_{D2}, 100 V / div.
Time: 200 ms / div.

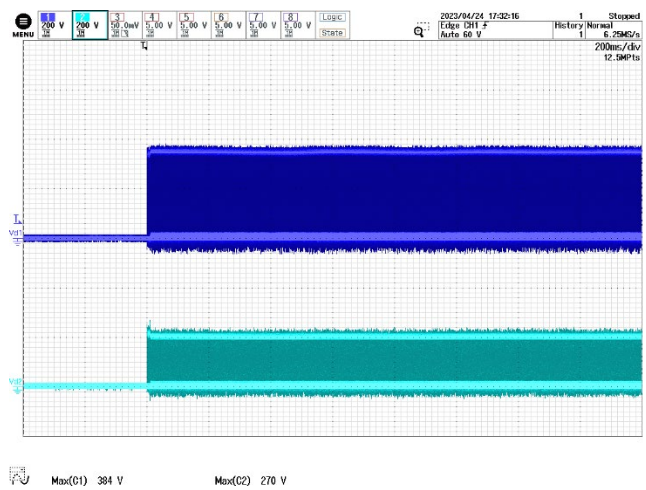


Figure 36 – Freewheeling Diode Voltages.
550 V_{DC}, 650 mA Load.
CH1: V_{D1}, 200 V / div.
CH2: V_{D2}, 200 V / div.
Time: 200 ms / div.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 105 °C Ambient Temperature

11.2.1.1 Normal Operation Component Stress

Steady-State Switching Waveforms 105 °C Ambient, Full Load						
Input	**LNK3209GQ**		**Freewheeling Diode 1**		**Freewheeling Diode 2**	
V_{IN} (V)	**IC1 V_{DS} (V)**	**V_{STRESS}(%)**	**D1 V_{DS} (V)**	**V_{STRESS}(%)**	**D2 V_{DS} (V)**	**V_{STRESS}(%)**
60	89.9	11.99	36.6	6.10	66.6	11.10
200	287	38.27	126	21.00	114	19.00
400	483	64.40	258.3	43.05	171	28.50
550	648	86.40	357	59.50	346.5	57.75

Table 9 – Summary of Critical Component Voltage Stresses at 105 °C Ambient Temperature.

11.2.1.2 LinkSwitch-TN2Q Drain Voltage and Current

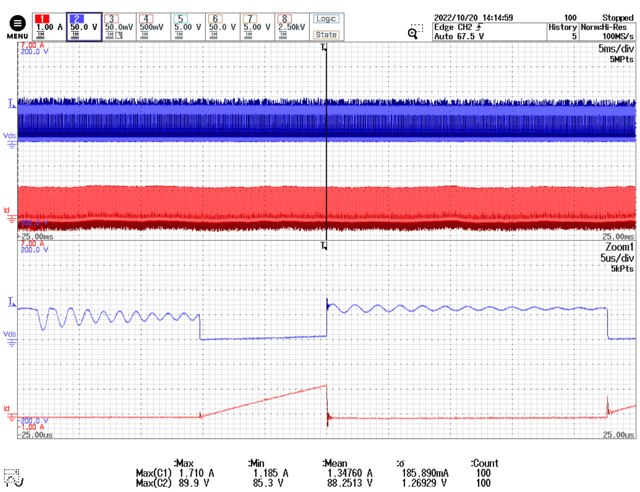


Figure 37 – LinkSwitch-TN2Q Drain Voltage and Current.
60 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH1: V_{DS}, 50 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

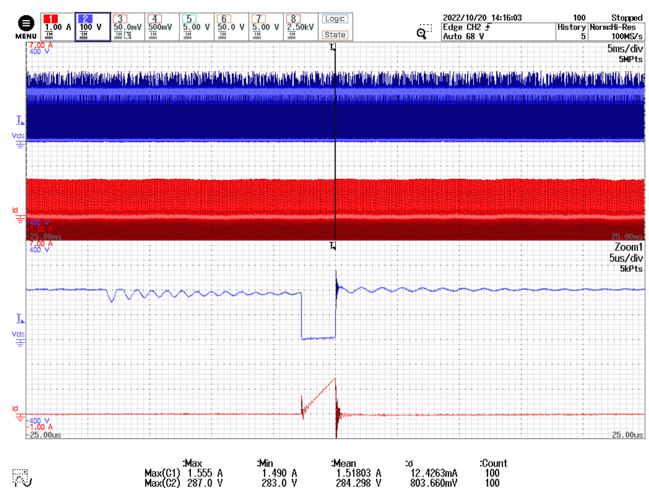


Figure 38 – LinkSwitch-TN2Q Drain Voltage and Current.
200 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH1: V_{DS}, 100 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

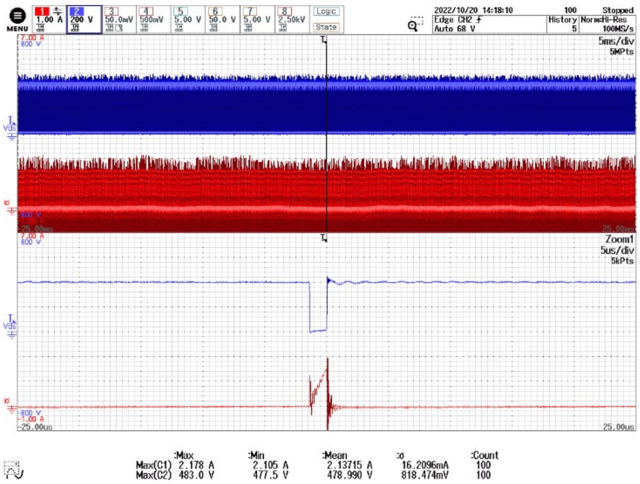


Figure 39 – LinkSwitch-TN2Q Drain Voltage and Current.
400 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH1: V_{DS}, 200 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

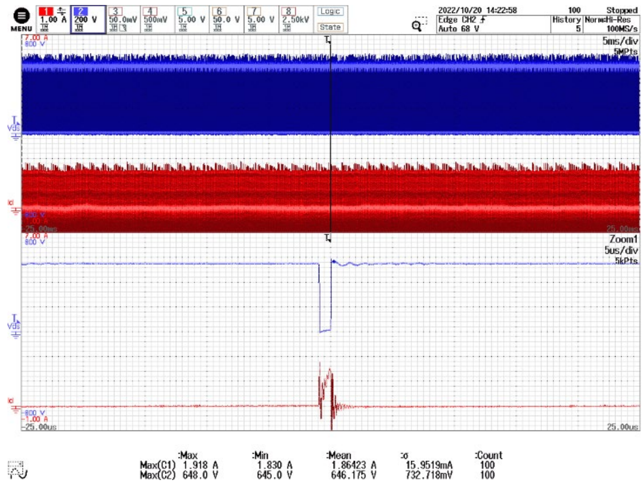


Figure 40 – LinkSwitch-TN2Q Drain Voltage and Current.
550 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH1: V_{DS}, 200 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

11.2.1.3 Freewheeling Diode Voltages

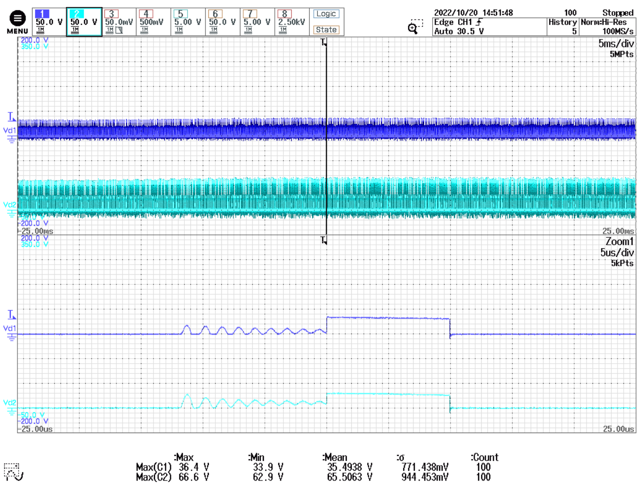


Figure 41 – Freewheeling Diode Voltages.
60 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: V_{D1}, 50 V / div.
CH1: V_{D2}, 50 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

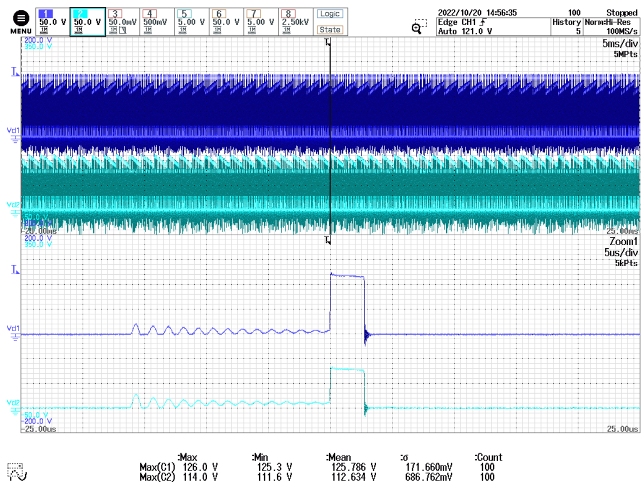


Figure 42 – Freewheeling Diode Voltages.
200 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: V_{D1}, 50 V / div.
CH1: V_{D2}, 50 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

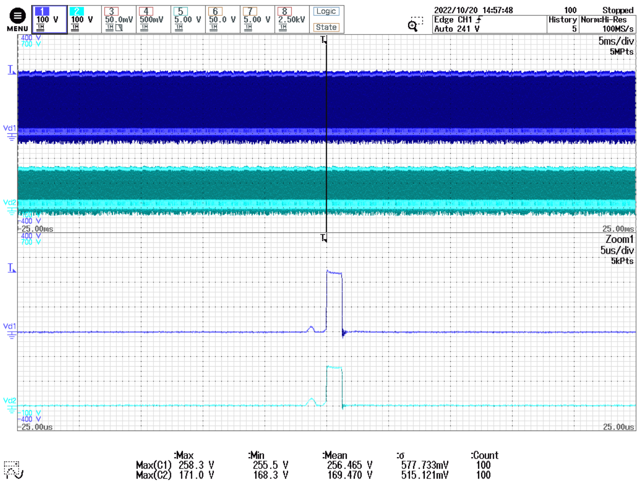


Figure 43 – Freewheeling Diode Voltages.
400 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: V_{D1}, 100 V / div.
CH1: V_{D2}, 100 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

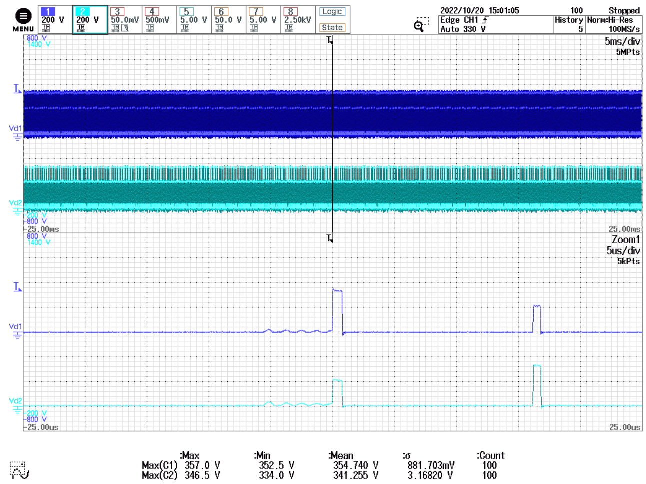


Figure 44 – Freewheeling Diode Voltages.
550 V_{DC}, 650 mA Load, 105 °C Ambient.
CH1: V_{D1}, 200 V / div.
CH1: V_{D2}, 200 V / div.
Time: 5 ms / div.
Zoom: 5 µs / div.

11.2.1.4 Short-Circuit Response

The unit is tested by applying output short-circuit across the 15 V_{DC} output terminals (X3A, X3B) during normal working conditions and then removing the short-circuit to see if the unit will recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto restart) mode.

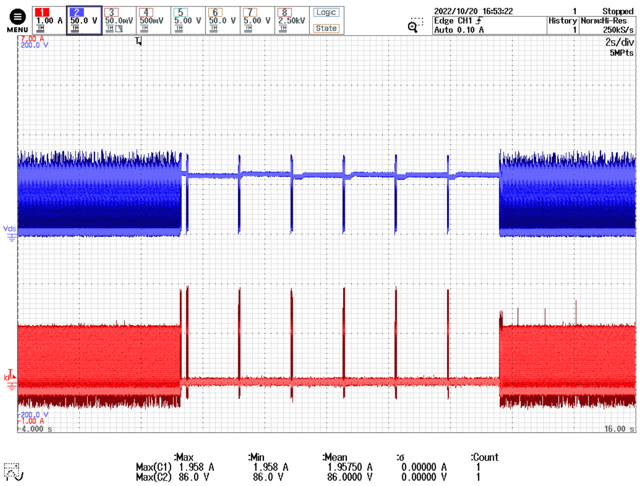


Figure 45 – LinkSwitch-TN2Q Drain Voltage and Current.
60 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH2: V_{VDS}, 50 V / div.
Time: 2 s / div.

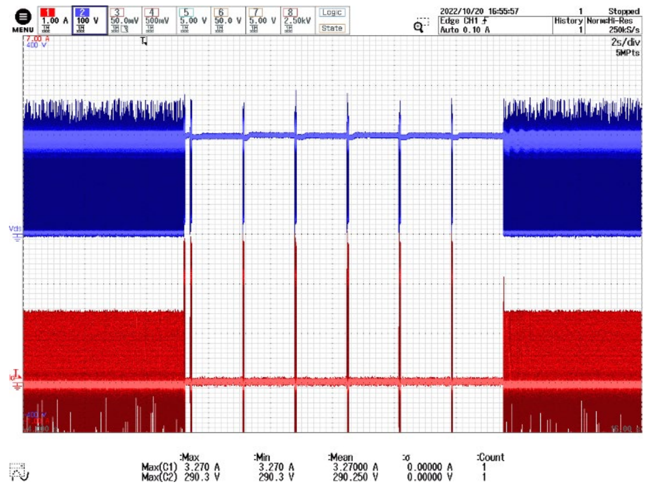


Figure 46 – LinkSwitch-TN2Q Drain Voltage and Current.
200 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH2: V_{VDS}, 100 V / div.
Time: 2 s / div.

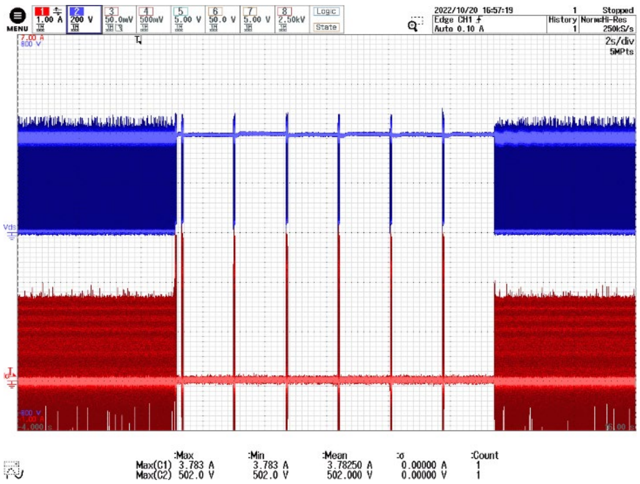


Figure 47 – LinkSwitch-TN2Q Drain Voltage and Current.
400 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH2: V_{VDS}, 200 V / div.
Time: 2 s / div.

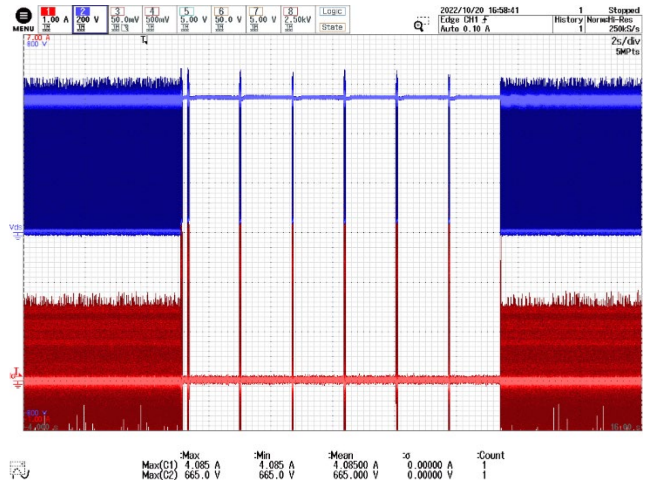


Figure 48 – LinkSwitch-TN2Q Drain Voltage and Current.
550 V_{DC}, Full Load-Short-Full Load, 105 °C Ambient.
CH1: I_D, 1 A / div.
CH2: V_{VDS}, 200 V / div.
Time: 2 s / div.

11.2.2 Switching Waveforms at 25 °C Ambient Temperature

11.2.2.1 LinkSwitch-TN2Q Drain Voltage and Current

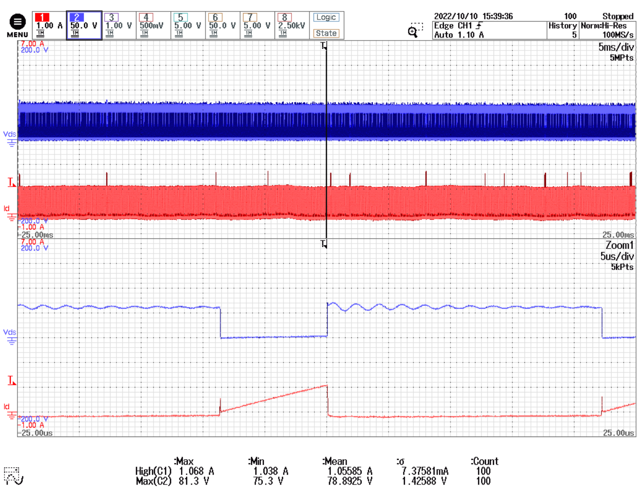


Figure 49 – LinkSwitch-TN2Q Drain Voltage and Current.
60 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 50 V / div.
Time: 5 ms / div.
Zoom: 5 μs / div.

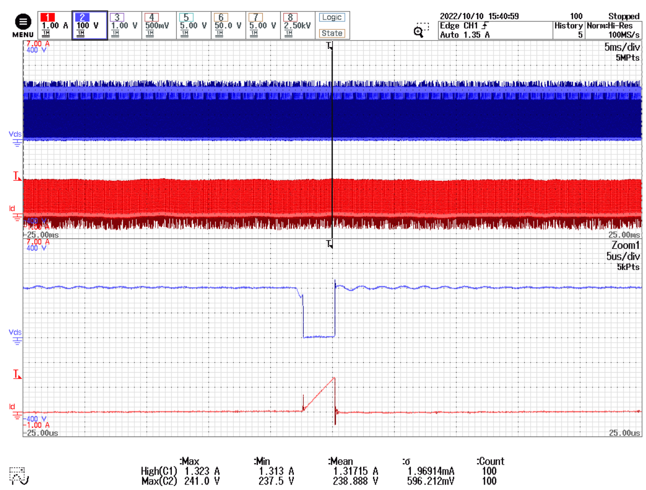


Figure 50 – LinkSwitch-TN2Q Drain Voltage and Current.
200 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 100 V / div.
Time: 5 ms / div.
Zoom: 5 μs / div.

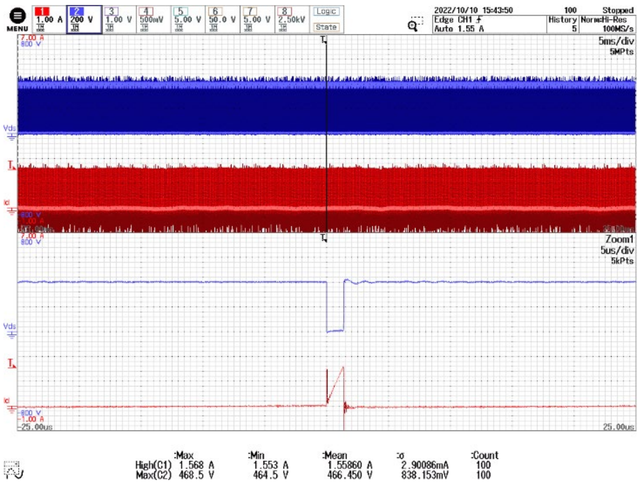


Figure 51 – LinkSwitch-TN2Q Drain Voltage and Current.
400 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 5 ms / div.
Zoom: 5 μs / div.

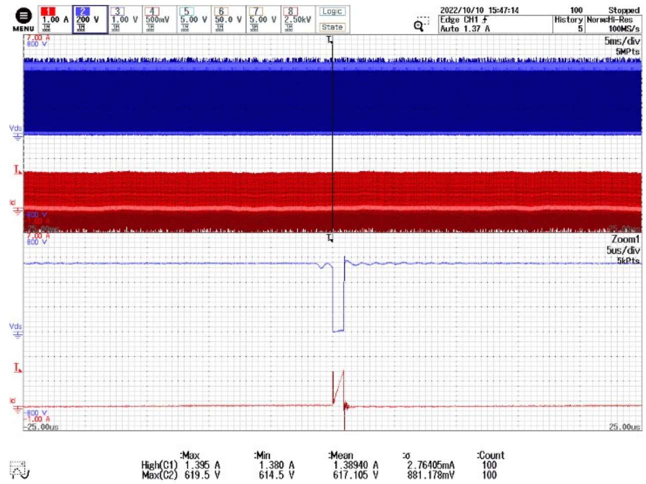


Figure 52 – LinkSwitch-TN2Q Drain Voltage and Current.
550 V_{DC}, 650 mA Load.
CH1: I_D, 1 A / div.
CH2: V_{DS}, 200 V / div.
Time: 5 ms / div.
Zoom: 5 μs / div.

11.2.2.2 Freewheeling Diode Voltages

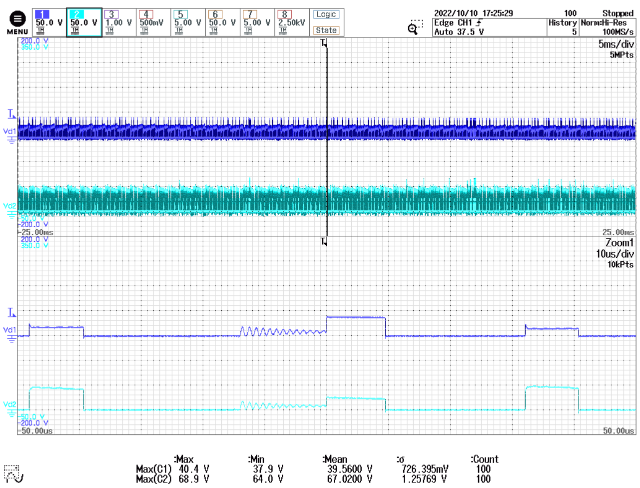


Figure 53 – Freewheeling Diode Voltages.
60 V_{DC}, 650 mA Load.
CH1: V_{D1}, 50 V / div.
CH2: V_{D2}, 50 V / div.
Time: 5 ms / div.
Zoom: 10 μs / div.

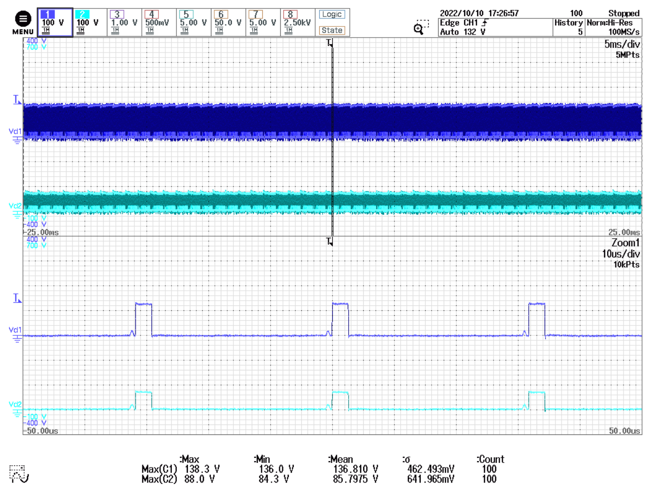


Figure 54 – Freewheeling Diode Voltages.
200 V_{DC}, 650 mA Load.
CH1: V_{D1}, 100 V / div.
CH2: V_{D2}, 100 V / div.
Time: 5 ms / div.
Zoom: 10 μs / div.

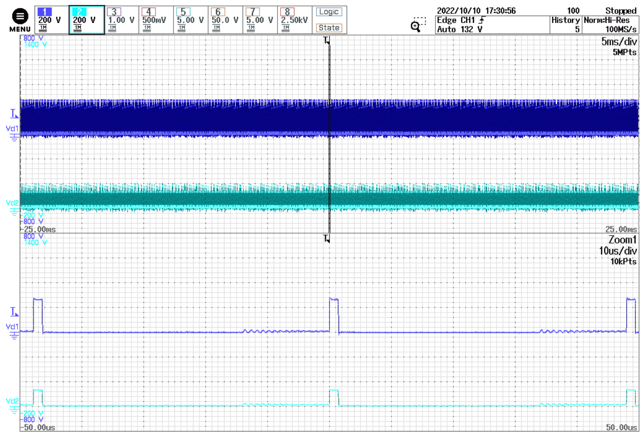


Figure 55 – Freewheeling Diode Voltages.
400 V_{DC}, 650 mA Load.
CH1: V_{D1}, 200 V / div.
CH2: V_{D2}, 200 V / div.
Time: 5 ms / div.
Zoom: 10 µs / div.

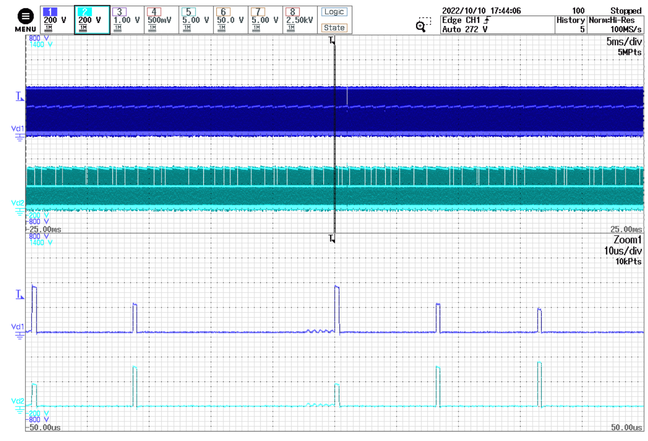


Figure 56 – Freewheeling Diode Voltages.
550 V_{DC}, 650 mA Load.
CH1: V_{D1}, 200 V / div.
CH2: V_{D2}, 200 V / div.
Time: 5 ms / div.
Zoom: 10 µs / div.

11.3 Load Transient Response

Output voltage waveform on the board was captured with dynamic load transient from 10% to 50%, 50% to 100%, and 10% to 100%. The duration for the load states is set to 100 ms and the load slew rate is 100 mA / µs. The test is done at 105 °C ambient temperature.

Dynamic Load Settings	V_{IN} (V)	ΔV_{OUT} (mV)	$V_{OUT(MIN)}$ (V)	$V_{OUT(MAX)}$ (V)
10% to 50%	60	514.00	15.30	15.81
	200	591.38	15.20	15.79
	400	554.25	15.22	15.78
	550	587.88	15.18	15.77
50% to 100%	60	435.50	15.17	15.60
	200	464.75	15.13	15.59
	400	545.50	14.97	15.51
	550	684.25	15.91	15.59
10% to 100%	60	686.00	15.14	15.82
	200	833.13	14.96	15.79
	400	972.38	14.82	15.79
	550	999.13	14.79	15.79

Table 10 – Load Transient Response.

11.3.1 10% to 50%

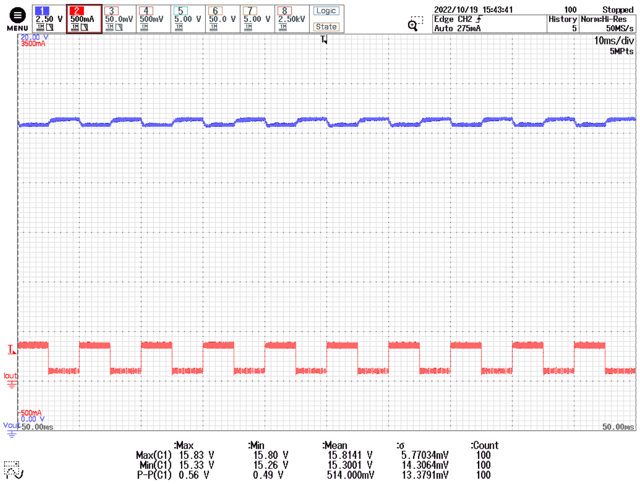


Figure 57 – Output Voltage and Current.
60 V_{DC}, 10% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 514 mV.

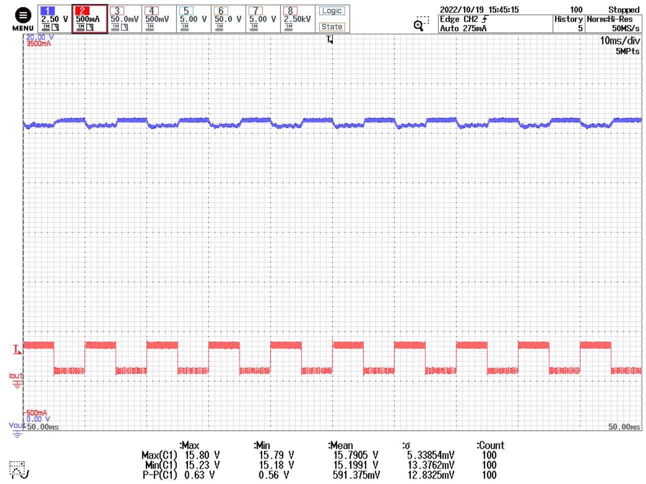


Figure 58 – Output Voltage and Current.
200 V_{DC}, 10% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 591.38 mV.

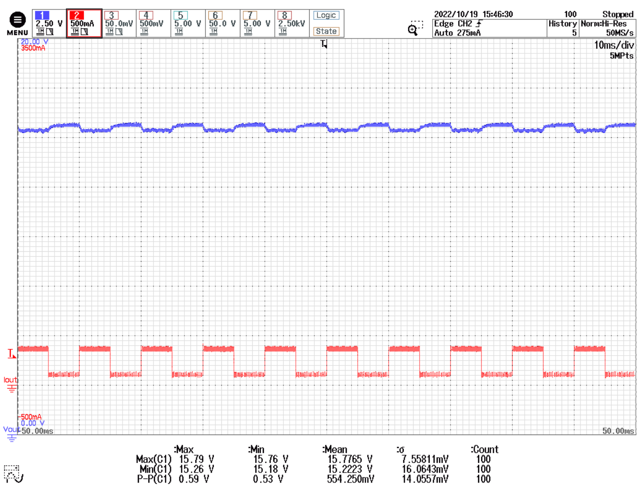


Figure 59 – Output Voltage and Current.
400 V_{DC}, 10% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 554.25 mV.

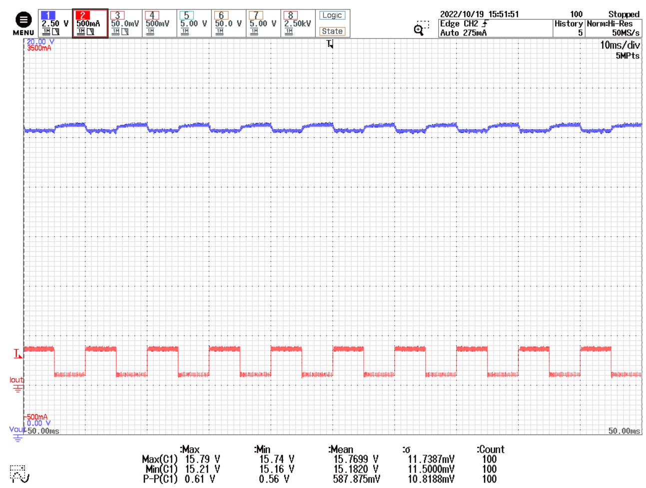


Figure 60 – Output Voltage and Current.
550 V_{DC}, 10% to 50% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 587.88 mV.

11.3.2 50% to 100%

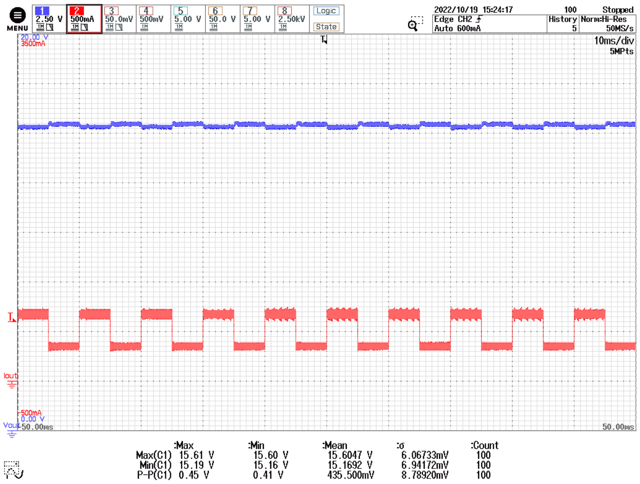


Figure 61 – Output Voltage and Current.
60 V_{DC}, 50% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 435.5 mV.

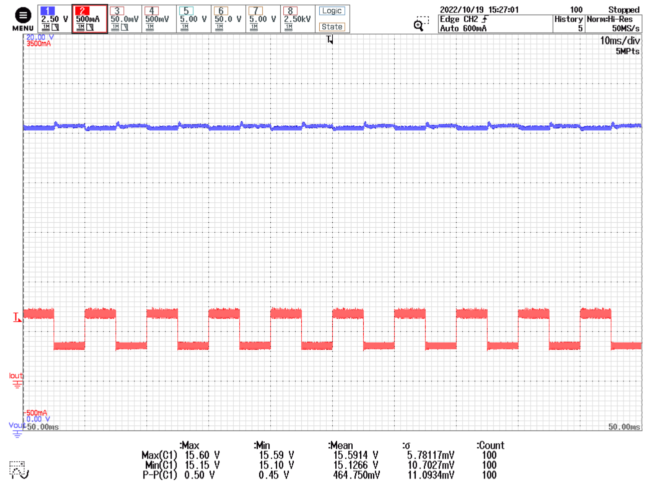


Figure 62 – Output Voltage and Current.
200 V_{DC}, 50% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 464.75 mV.

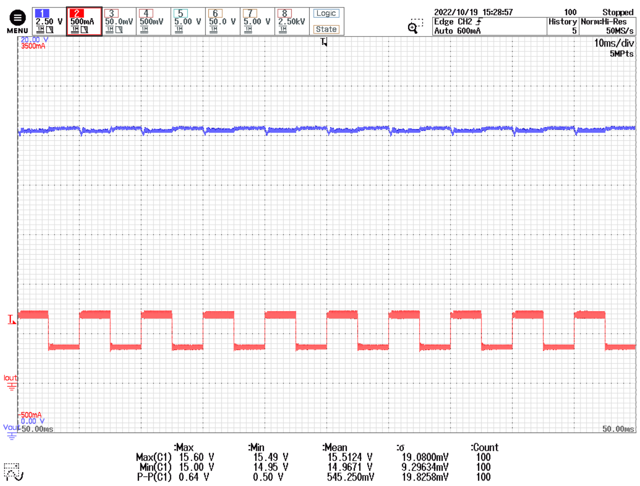


Figure 63 – Output Voltage and Current.
400 V_{DC}, 50% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 545.50 mV.

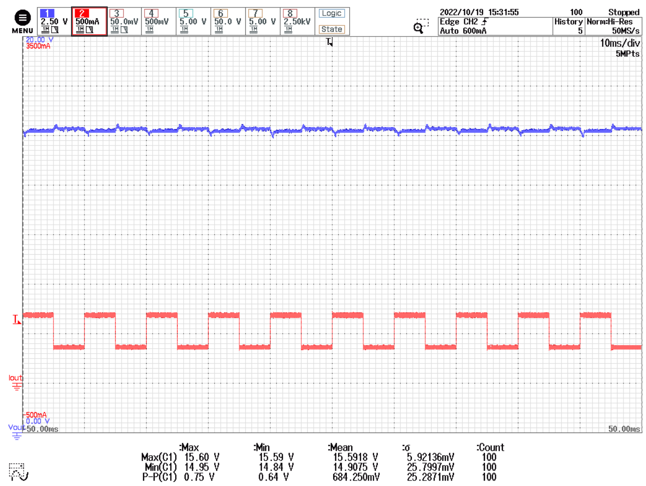


Figure 64 – Output Voltage and Current.
550 V_{DC}, 50% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 684.25 mV.

11.3.3 10% to 100%

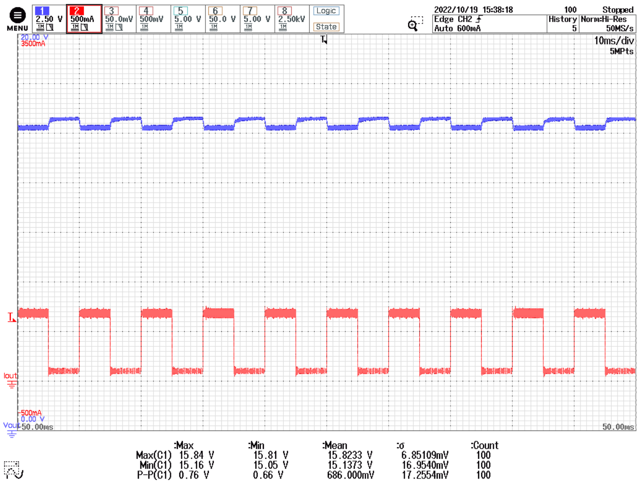


Figure 65 – Output Voltage and Current.
60 V_{DC}, 10% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 686.00 mV.

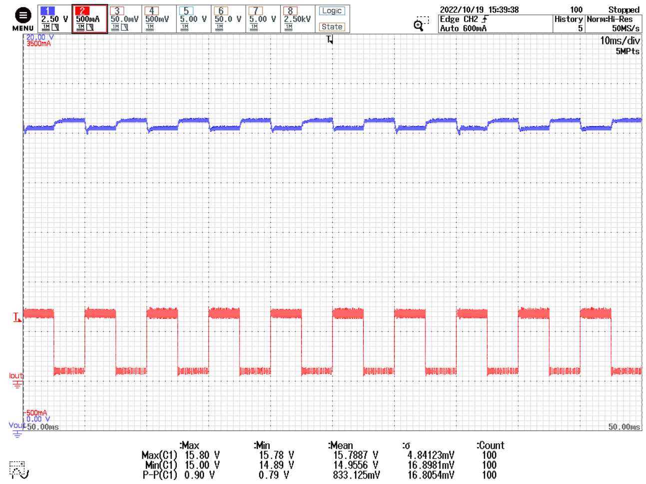


Figure 66 – Output Voltage and Current.
200 V_{DC}, 10% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 833.13 mV.

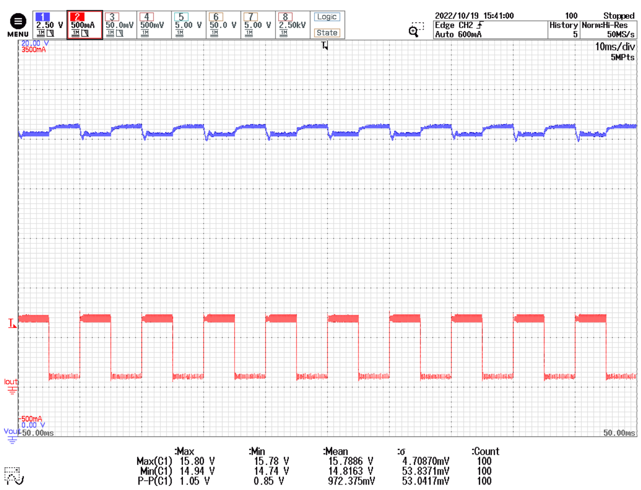


Figure 67 – Output Voltage and Current.
400 V_{DC}, 10% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 972.38 mV.

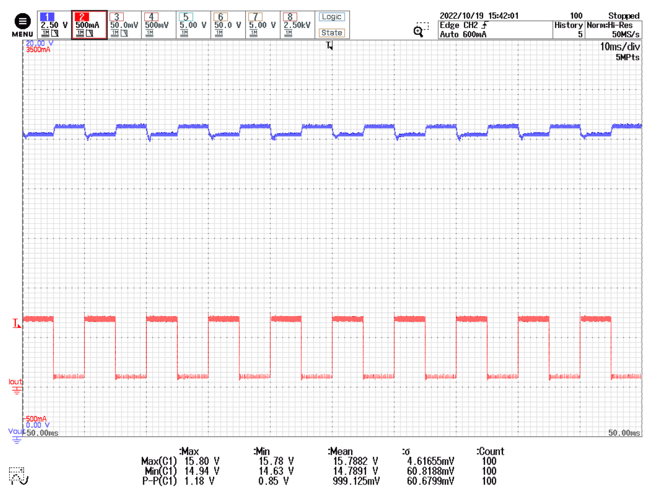


Figure 68 – Output Voltage and Current.
550 V_{DC}, 10% to 100% Transient Load,
105 °C Ambient.
CH1: V_{OUT}, 2.5 V / div.
CH2: I_{OUT}, 500 mA / div.
Time: 10 ms / div.
ΔV = 999.13 mV.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 69 and Figure 70 below.

A CT2708 probe adapter is affixed with a 1 μF / 50 V ceramic capacitor placed in parallel across the probe tip. A twisted pair of wires kept as short as possible is soldered directly to the probe and the output terminals.

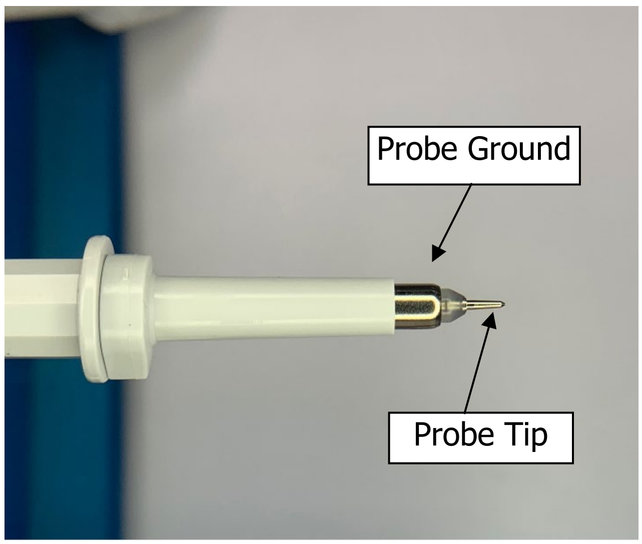


Figure 69 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

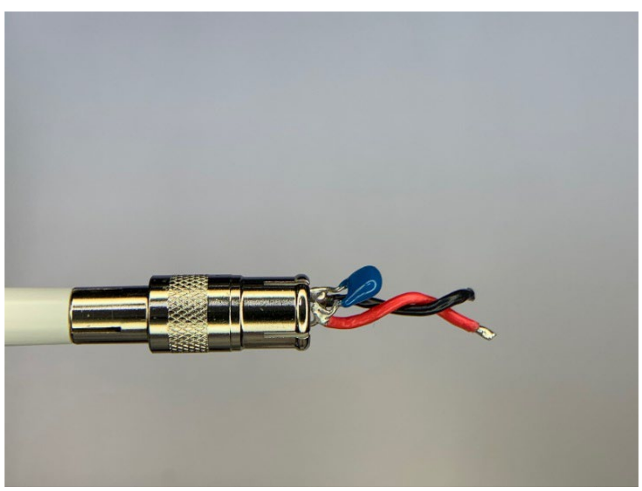


Figure 70 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 105 °C Ambient[10]

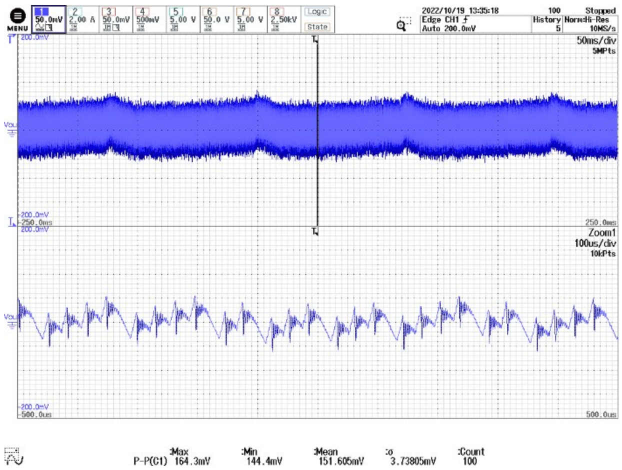


Figure 71 – Output Voltage Ripple.
60 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 151.61 mV.

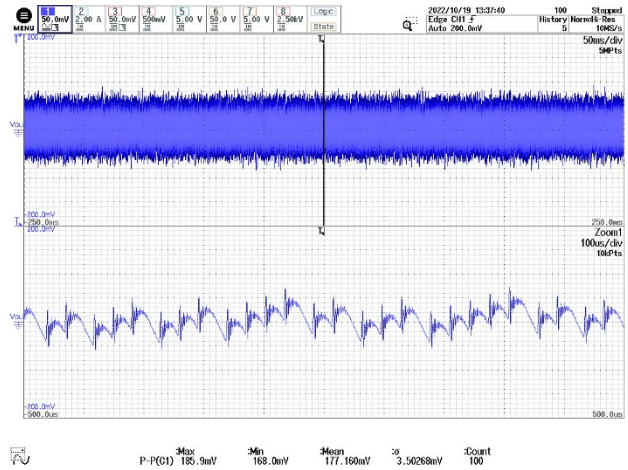


Figure 72 – Output Voltage Ripple.
200 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 177.16 mV.

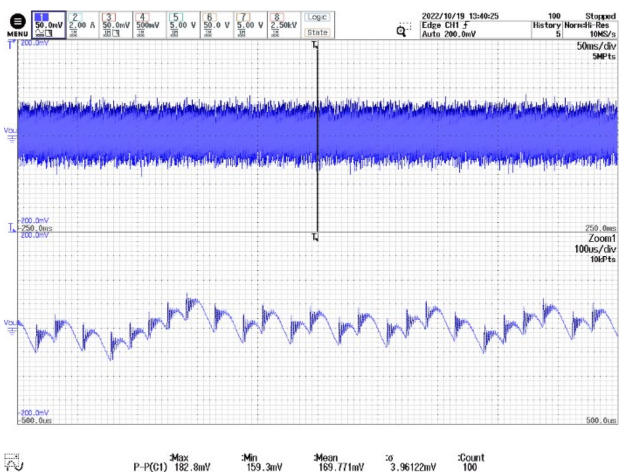


Figure 73 – Output Voltage Ripple.
400 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 169.77 mV.

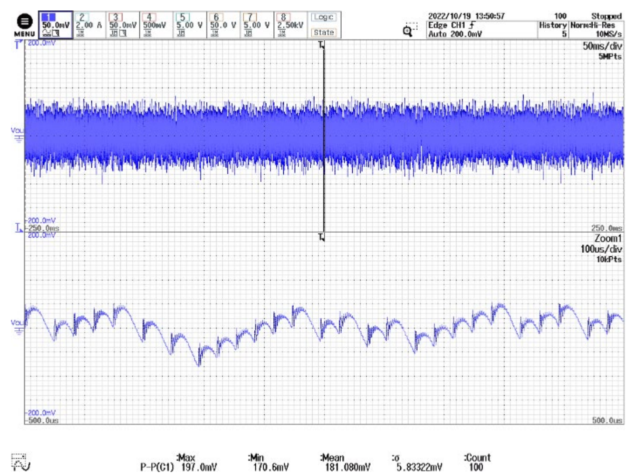


Figure 74 – Output Voltage Ripple.
550 V_{DC}, Full Load, 105 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 181.08 mV.

[10] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient[11]

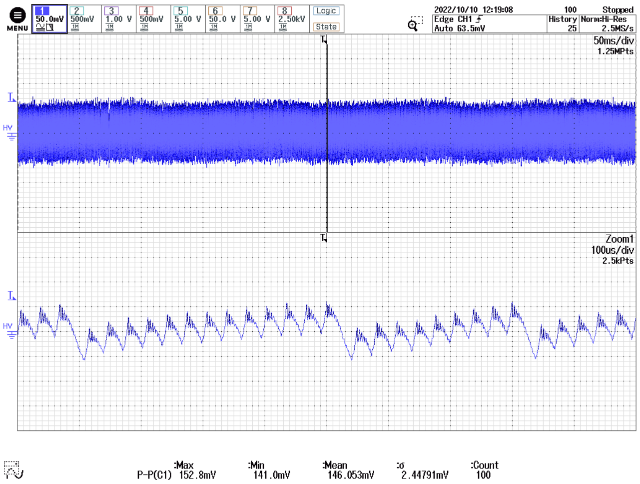


Figure 75 – Output Voltage Ripple.
60 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 µs / div.
V_{RIPPLE} = 146.05 mV.

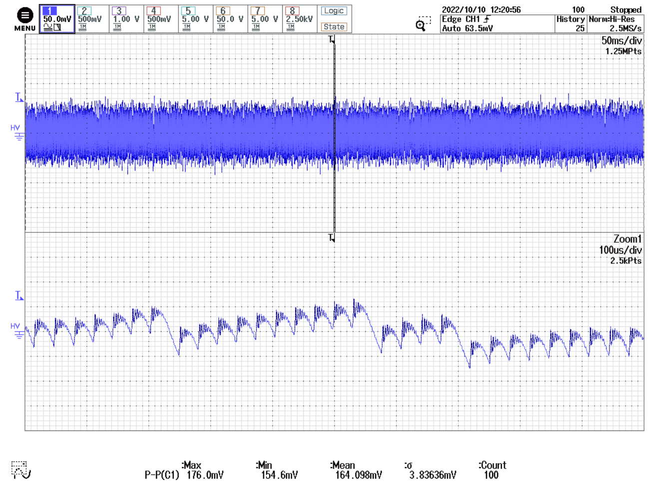


Figure 76 – Output Voltage Ripple.
200 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 µs / div.
V_{RIPPLE} = 164.10 mV.

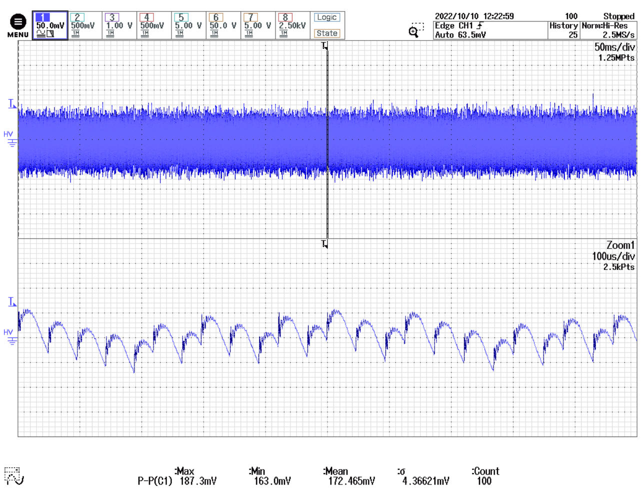


Figure 77 – Output Voltage Ripple.
400 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 µs / div.
V_{RIPPLE} = 172.47 mV.

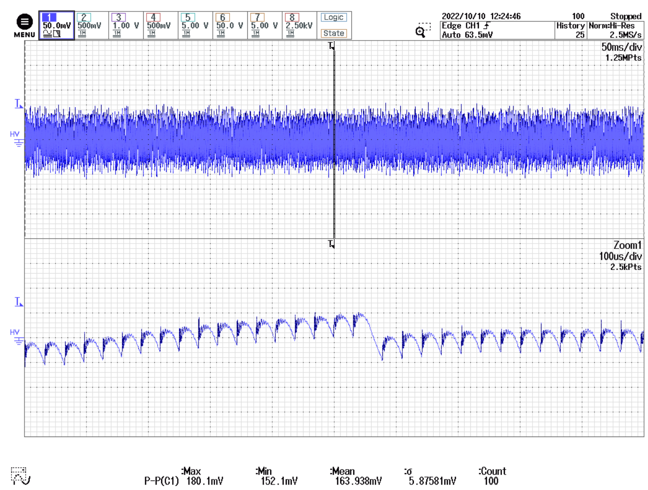


Figure 78 – Output Voltage Ripple.
550 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 µs / div.
V_{RIPPLE} = 163.94 mV.

[11] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient[12]

Probe extension using twisted pair wires was implemented for the test performed at -40 °C ambient temperature due to the inaccessibility of the probing point once placed inside the thermal chamber. To compensate for the effects of the probe extension, values shown on the figures below must be decreased by 11.44 mV_{PP}[13].

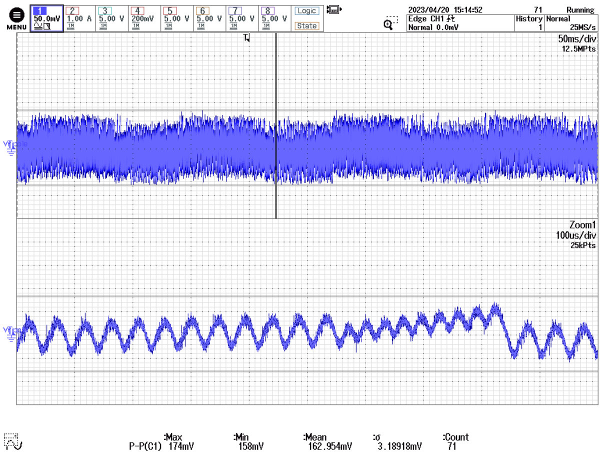


Figure 79 – Output Voltage Ripple.
60 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 162.95 mV.

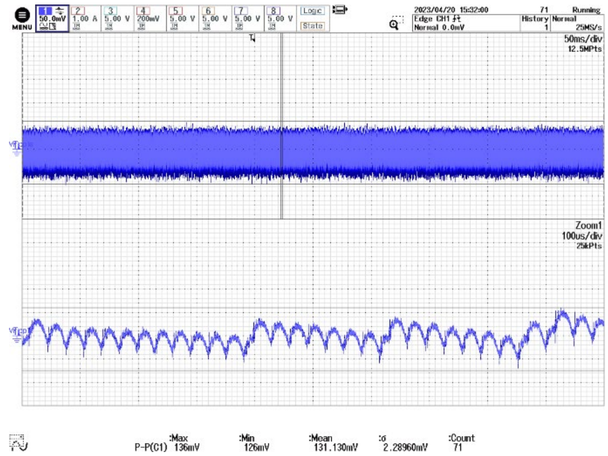


Figure 80 – Output Voltage Ripple.
200 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 131.13 mV.

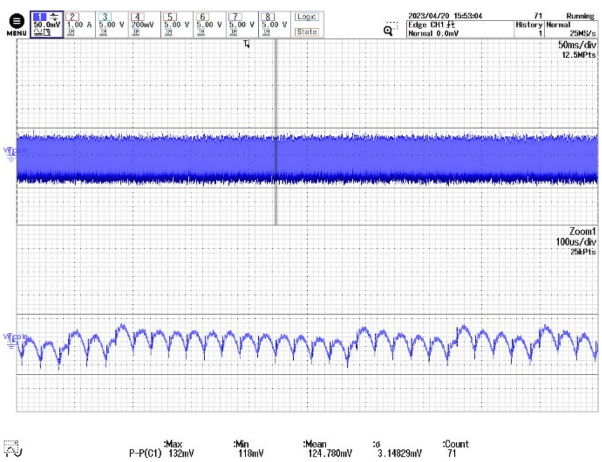


Figure 81 – Output Voltage Ripple.
400 V_{DC}, Full Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 124.78 mV.

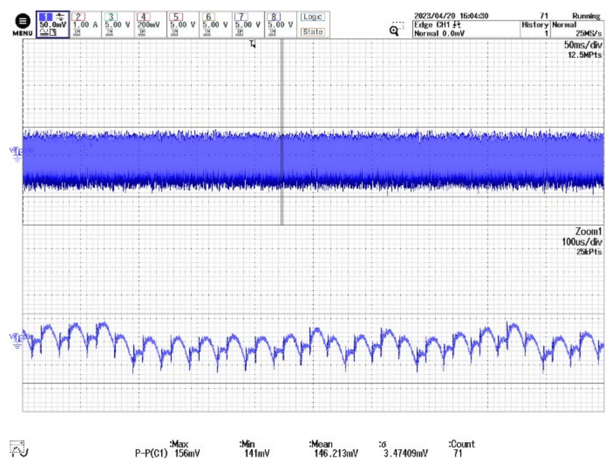


Figure 82 – Output Voltage Ripple.
550 V_{DC}, Full Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 50 ms / div.
Zoom: 100 μs / div.
V_{RIPPLE} = 146.21 mV.

[12] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).
[13] 11.44 mV_{PP} is the average value of the difference between the output voltage ripple measurement obtained while using a short and extended probe at 25 °C ambient temperature.

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 105 °C Ambient

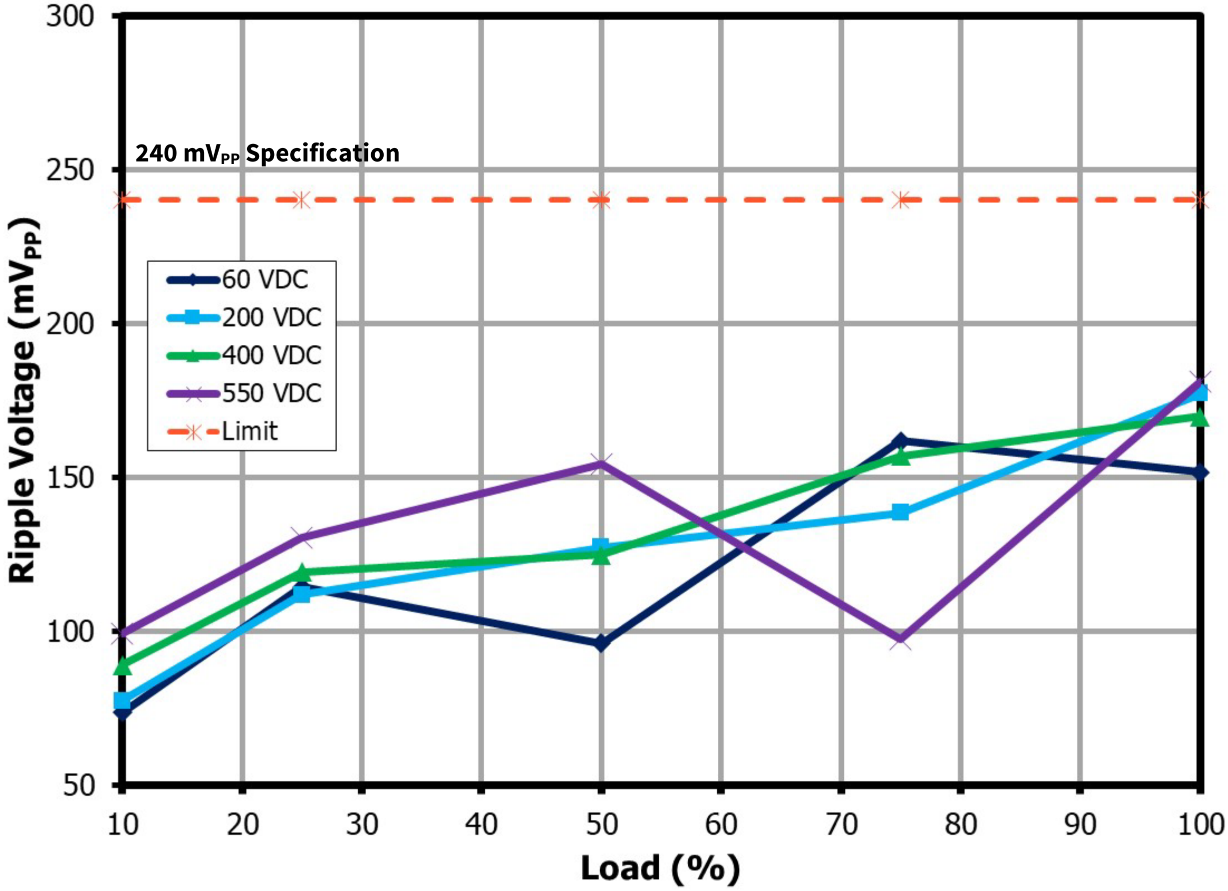


Figure 83 – Output Ripple Voltage (105 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

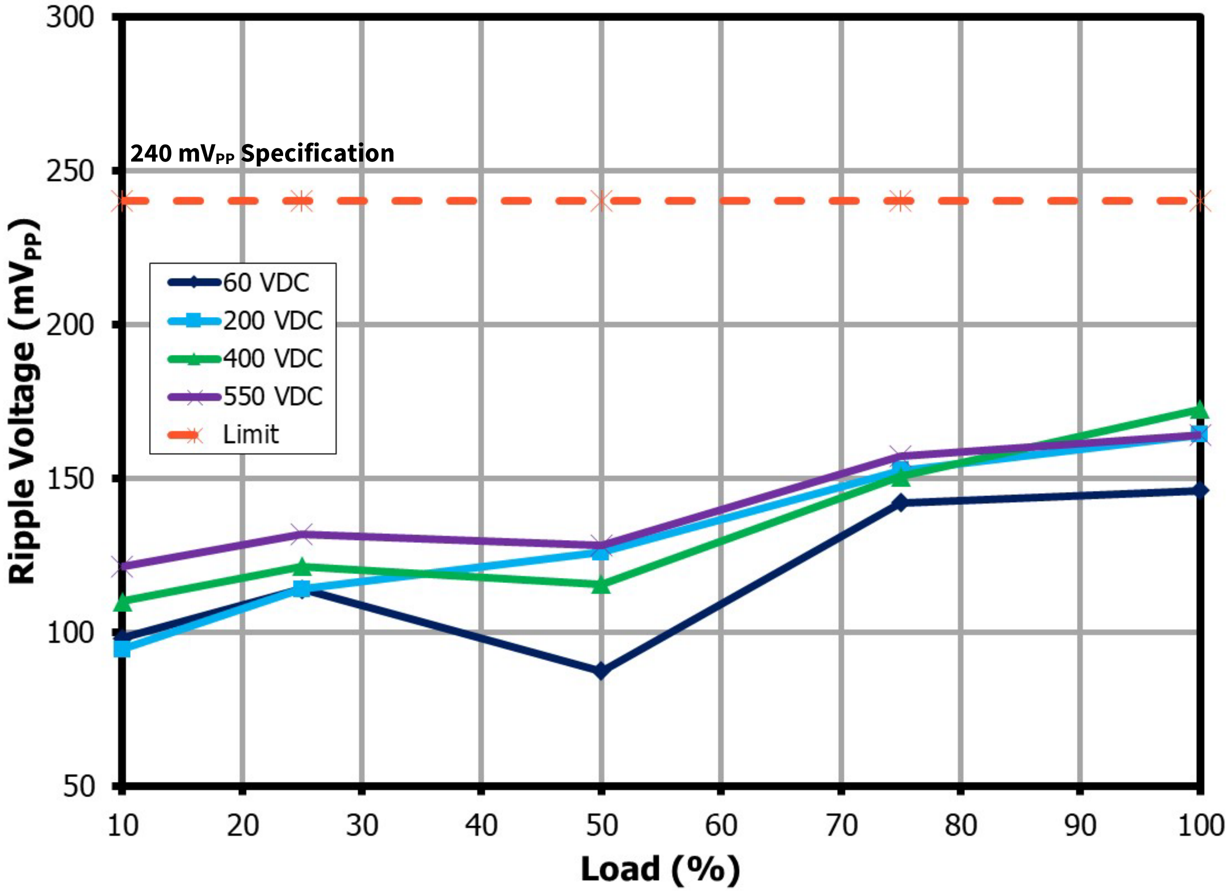


Figure 84 – Output Ripple Voltage (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

Output voltage ripple data at -40 °C ambient temperature shown below includes the 11.44 mV_{PP}[14] offset to compensate for the effect the probe extensions had on the voltage ripple values.

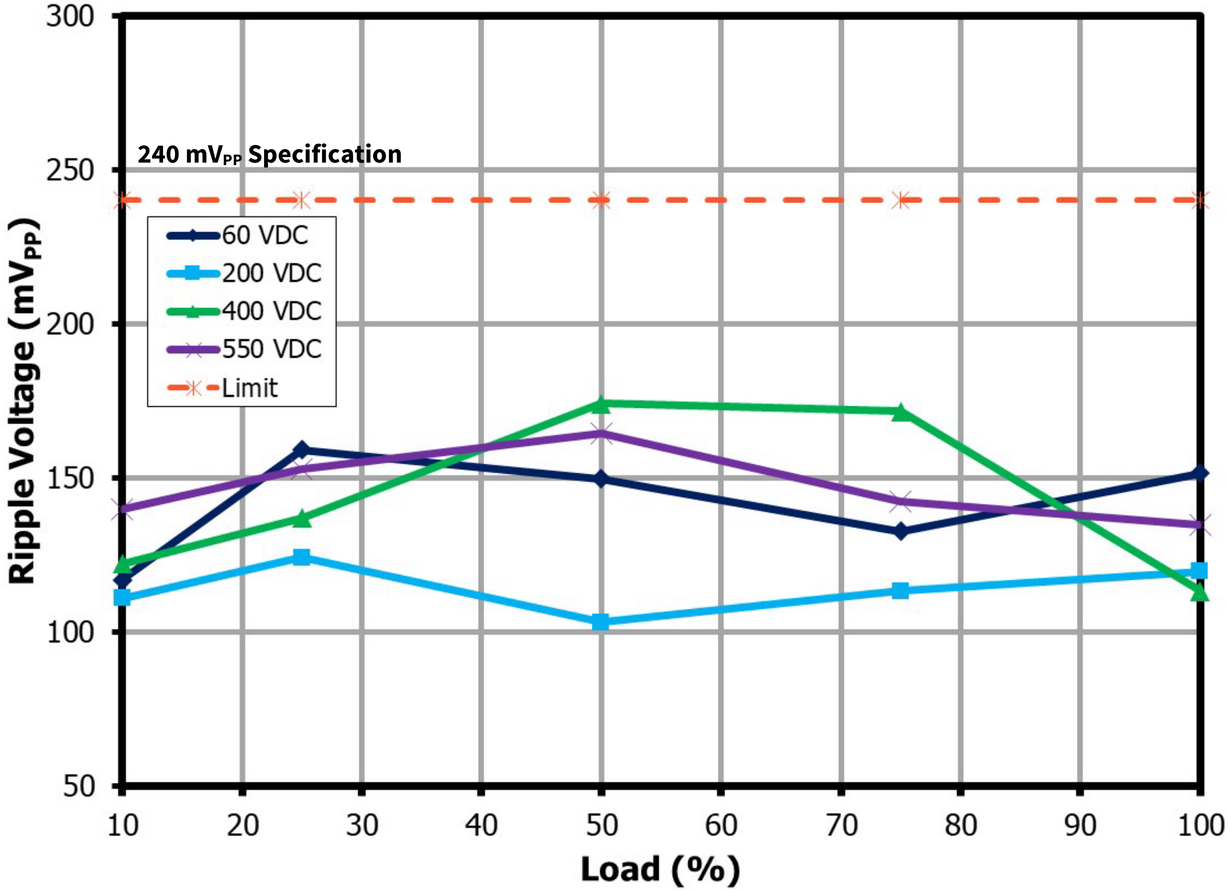


Figure 85 – Output Ripple Voltage (-40 °C Ambient).

[14] 11.44 mV_{PP} is the average value of the difference between the output voltage ripple values obtained while using a short and extended probe at 25 °C ambient temperature.

11.5 Output Voltage Response due to Dynamic Inputs

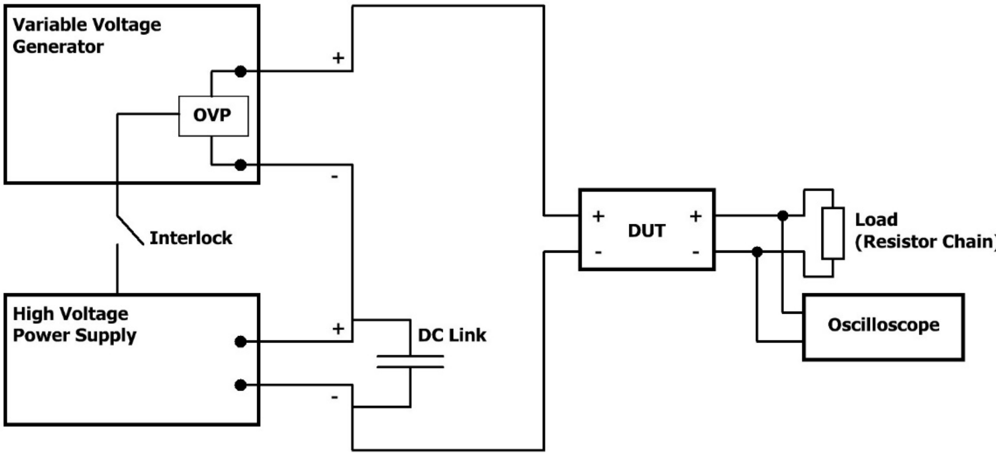


Figure 86 – Test Set-up Diagram.

11.5.1 Response to HV DC Ramp Up with Ripple

To test the output voltage response due to ripple at HV DC ramp up, the input voltage was ramped up from 0 V to 60 V at 100 V / s and 50 V / s. A ripple modulation of ±8 V was implemented on the input voltage using a Variable Voltage Generator. Waveforms were obtained under minimum load (I_{OUT} = 65 mA) and full load (I_{OUT} = 650 mA) conditions.

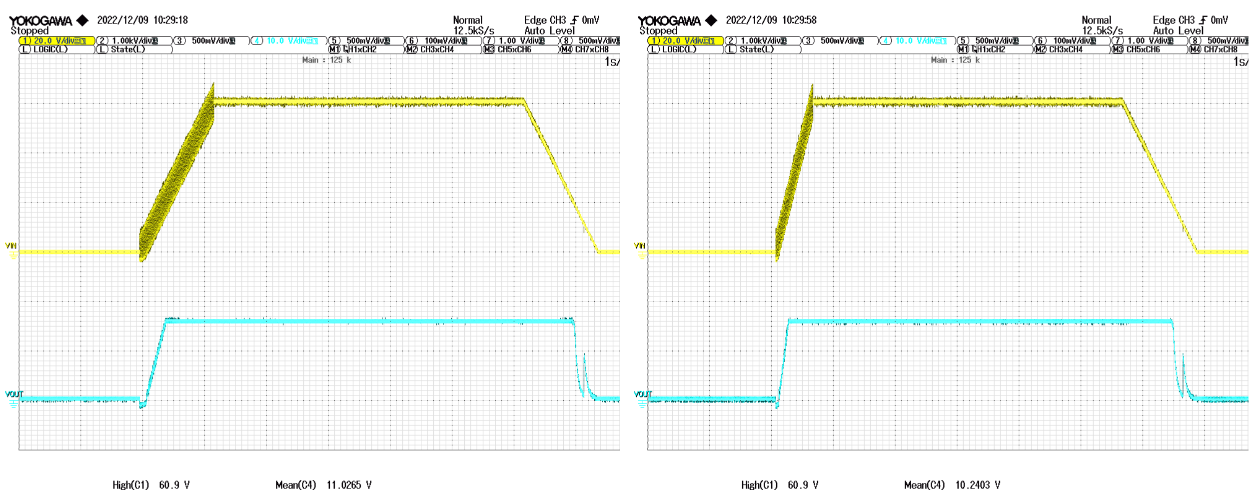


Figure 87 – 50 V / s Ramp Up (Left) and 100 V / s Ramp Up (Right).
0 – 60 V_{DC}, 65 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 20 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 1 s / div.

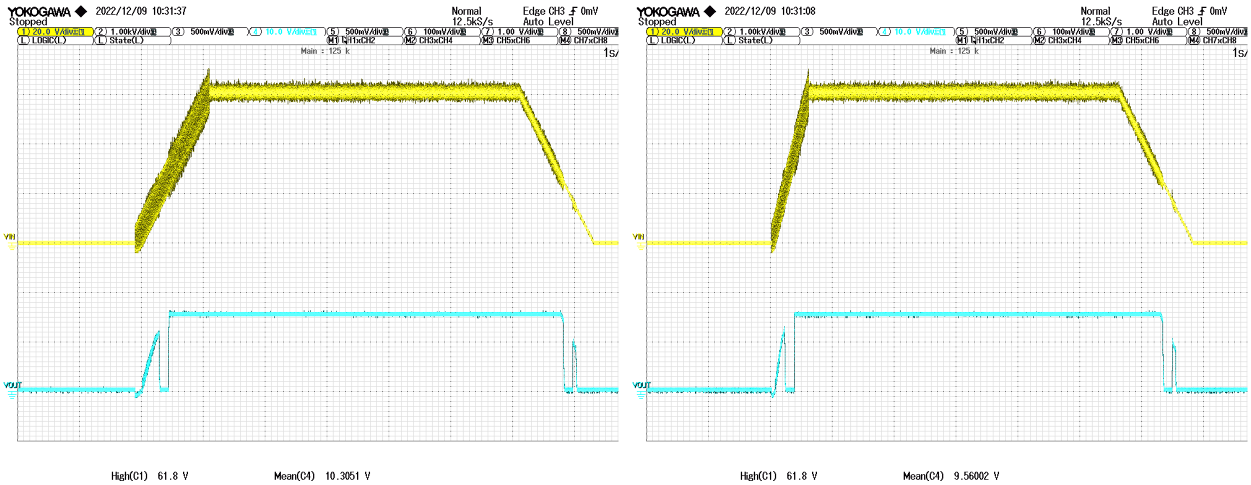


Figure 88 – 50 V / s Ramp Up (Left) and 100 V / s Ramp Up (Right).
0 – 60 V_{DC}, 650 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 20 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 1 s / div.

The waveforms from Figure 87 and Figure 88 show no influence on the output voltage caused by the ripple modulation on the input voltage. The triggering of the "auto-restart" (AR) feature observed during the input voltage ramp up at full load condition and ramp down at both loading conditions is expected to happen when the output voltage regulation is not reached within a 50 ms period.

11.5.2 Response to Ripple on HV DC Net

11.5.2.1 Severity Level 1 Ripple on HV DC Net

A severity level 1 ripple was applied on the input voltage after 10 minutes of running the unit at normal operation to test the unit's output voltage response to ripple on the HV DC net. Waveforms were obtained under minimum load (I_{OUT} = 65 mA) and full load (I_{OUT} = 650 mA) conditions.

A severity level 1 ripple is a ripple profile with voltage ripple magnitudes of ±0.5 V to ±8 V and increasing frequency from 15 Hz to 200 kHz. The parameters implemented for the test performed are usual customer specifications.

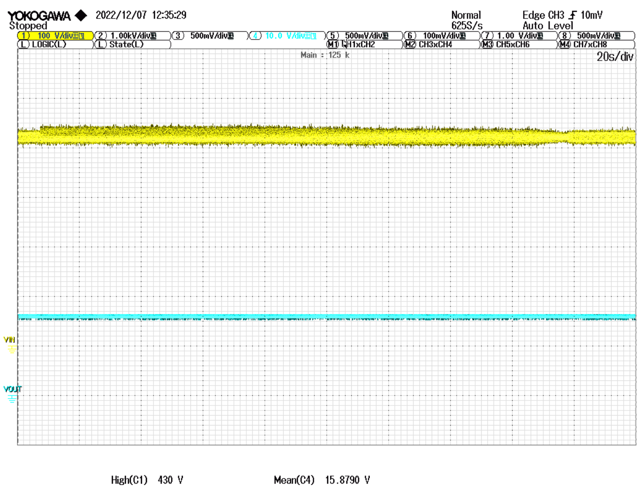


Figure 89 – Severity Level 1 on HVDC Net.
420 V_{DC}, 65 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 100 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 20 s / div.

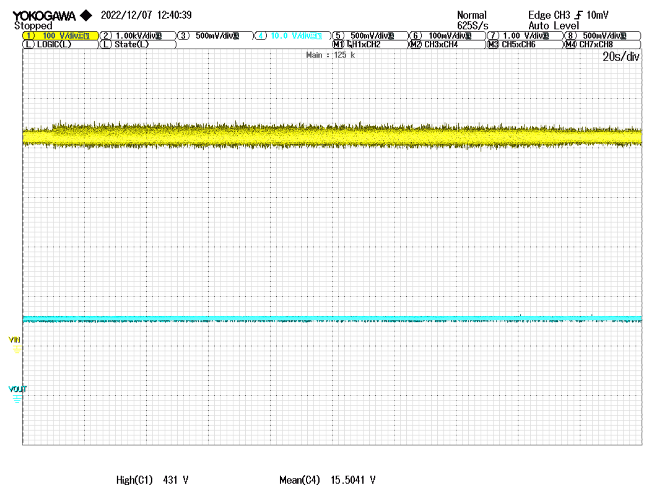


Figure 90 – Severity Level 1 on HVDC Net.
420 V_{DC}, 650 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 100 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 20 s / div.

The waveforms from Figure 89 and Figure 90 show no influence on the output voltage caused by the 420 V_{DC} input voltage with a severity level 1 ripple.

11.5.2.2 Severity Level 2 Ripple Definition on HV DC Net

A severity level 2 ripple was applied on the input voltage after 10 minutes of running the unit at normal operation to test the unit's output voltage response to ripple on the HV DC net. Waveforms were obtained under minimum load (I_{OUT} = 65 mA) and full load (I_{OUT} = 650 mA) conditions.

A severity level 2 ripple is a ripple profile with voltage ripple magnitudes of ±0.5 V to ±16 V and increasing frequency from 15 Hz to 200 kHz. The parameters implemented for the test performed are usual customer specifications.

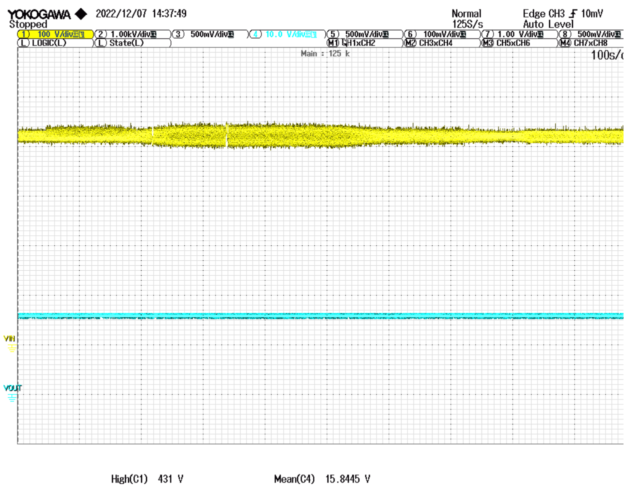


Figure 91 – Severity Level 2 on HVDC Net.
420 V_{DC}, 65 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 100 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 20 s / div.

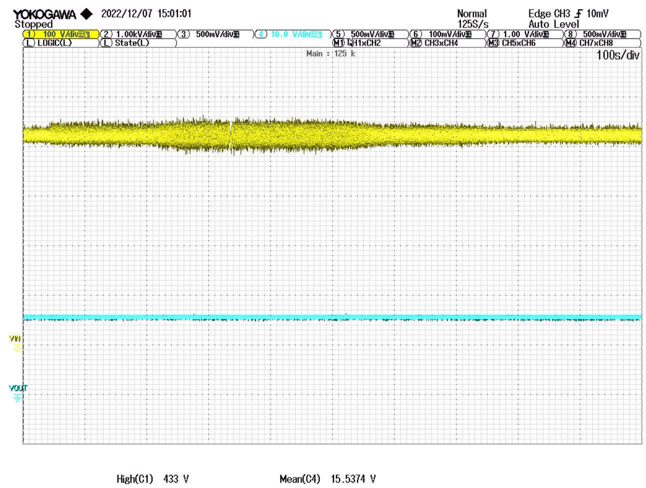


Figure 92 – Severity Level 2 on HVDC Net.
420 V_{DC}, 650 mA Load, 25 °C Ambient.
CH 1: V_{IN}, 100 V / div.
CH 4: V_{OUT}, 10 V / div.
Time: 20 s / div.

The waveforms from Figure 91 and Figure 92 show no influence on the output voltage caused by the 420 V_{DC} input voltage with a severity level 2 ripple modulation.

12 Revision History

Date	Author	Revision	Description & Changes	Reviewed
07-Feb-23	JB	1.0	Initial Release.	Apps & Mktg
09-Jul-23	JS	2.0	Updated and added sections and figures for the data at -40 °C ambient temperature test condition.	Apps & Mktg

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